Power Management ICs for Handheld Device

General Description

The RT9941 is a complete power management IC (PMIC) for handheld device platform. This PMIC contains a fully integrated linear charger for a single cell Lithium Ion battery, five LDO linear regulators and two high efficiency buck converters, a comparator, a reset and an I^2C serial interface to program one buck and one regulator output voltages as well as power on timing control for complete flexibility.

The linear charger integrates LDO, MOSFET pass element and thermal-regulation circuitry. The proprietary thermal-regulation circuitry limits the die temperature when fast charging or while exposed to high ambient temperatures, allowing maximum charging current without damaging the IC.

The two step-down converters are optimized for small size inductor and high efficiency applications. They utilize a proprietary hysteretic PWM control scheme that switches with nearly fixed frequency and is adjustable, allowing the customer to trade some efficiency for smaller external component as desired.

The LDO linear regulators provide high power supply rejection rate and have only $45\mu V_{RMS}$ of output noises for 100Hz to 10kHz frequency range to power noise sensitive RF sections.

The RT9941 is available in WQFN-40L 5x5 package.

Ordering Information

RT9941 □ □

- Package Type
  - QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

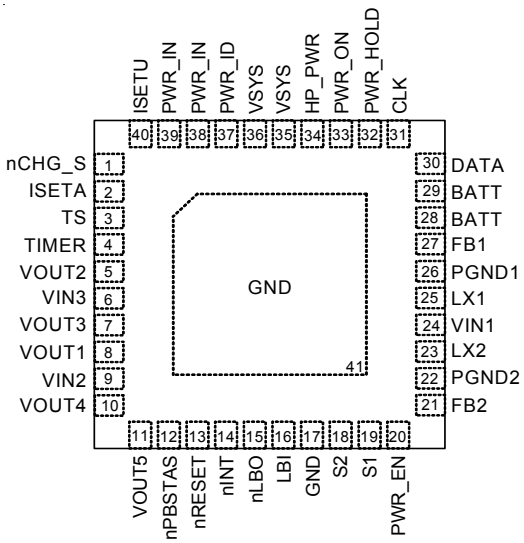
- **Charger**
  - **Adapter & Battery Two Input with Auto Power Dynamic Path.**
  - **PWR_IN LDO support continuous 1.5A, peak 2A current**
  - **4.5V to 5.5V Operation Voltage Range with Max. Input 18V from PWR_IN Pin**
  - **Switch Well for LDO and Charger Power MOSFET**
  - **Set Charge Current by ISETA Pin**
  - **Charge Status Indicator**
  - **Interrupt for PWR_IN Plug In/Out Time Out and Charger Done.**
  - **Battery Temperature Monitoring**
- **Hysteretic Buck**
  - **Buck 1 for DDR Memory, Adjustable Voltage and 600mA Output Current**
  - **Buck 2 for PDN with 25mV/step I^2C Adjustable 800mA Output Current**
  - **Max. Efficiency Up to 90%**
- **LDO**
  - **LDO1 : 3.3V/500mA for I/O, Default ON**
  - **LDO2 : 1.2V/80mA for PLL, Default ON**
  - **LDO3 : 1.2V/80mA for Pre-Core. I^2C Adiustable, Sync. with Buck2, Default ON**
  - **LDO4 : 2.5V/50mA for AVDD of USB, ADC, TSC, Default ON**
  - **LDO5 : 3.3V/50mA for AVDD of USB, Default ON**
  - **Minimize the External Component Counts**
- **Other**
  - **System Reset**
  - **Low Voltage Detector**
  - **I^2C Compatible Interface**
  - **Power ON Timing Control**
- **RoHS Compliant and Halogen Free**

Applications

- GPS and PDA
- Handheld Devices

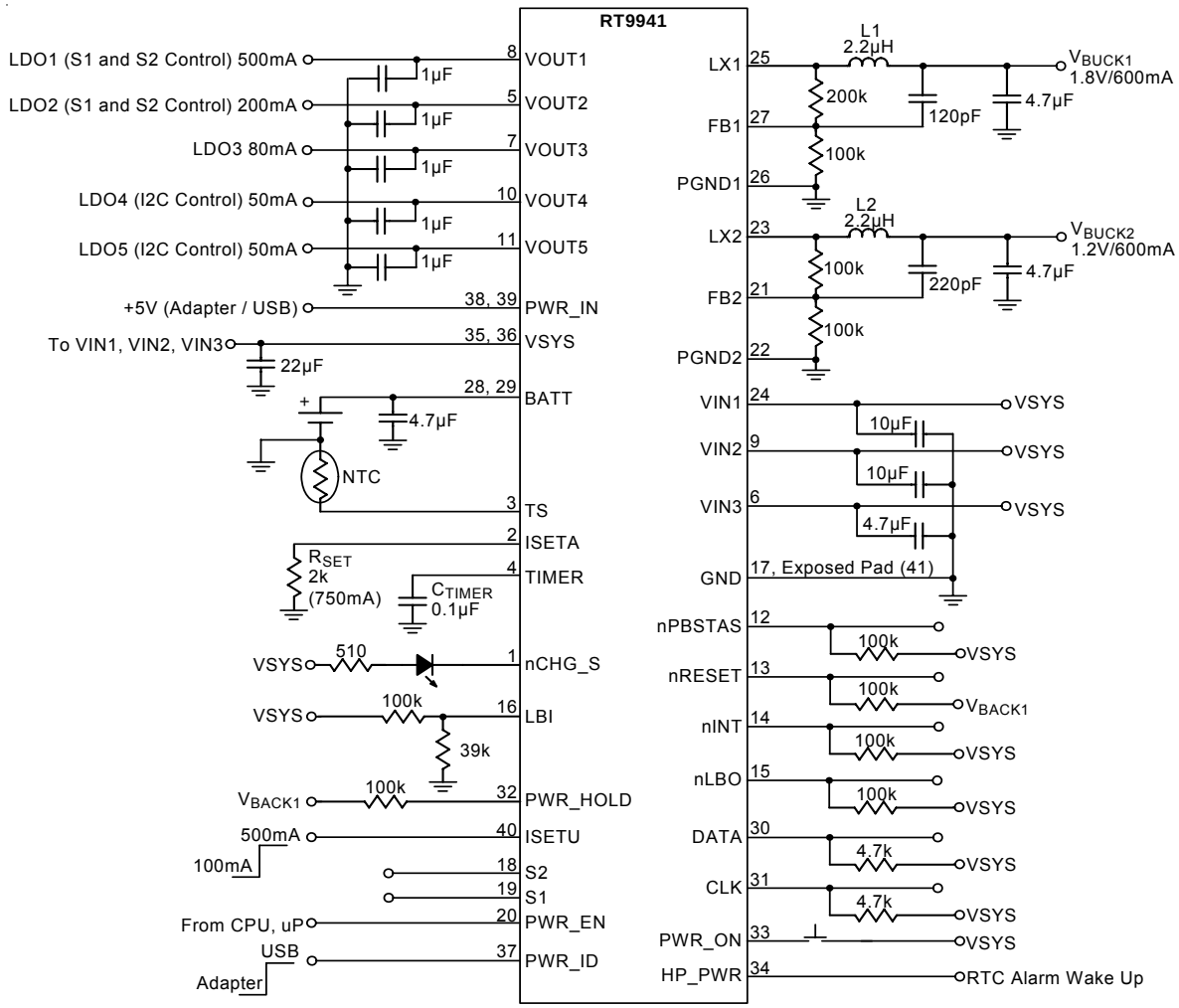
Pin Configurations

(TOP VIEW)



WQFN-40L 5x5

Typical Application Circuit



Functional Pin Description

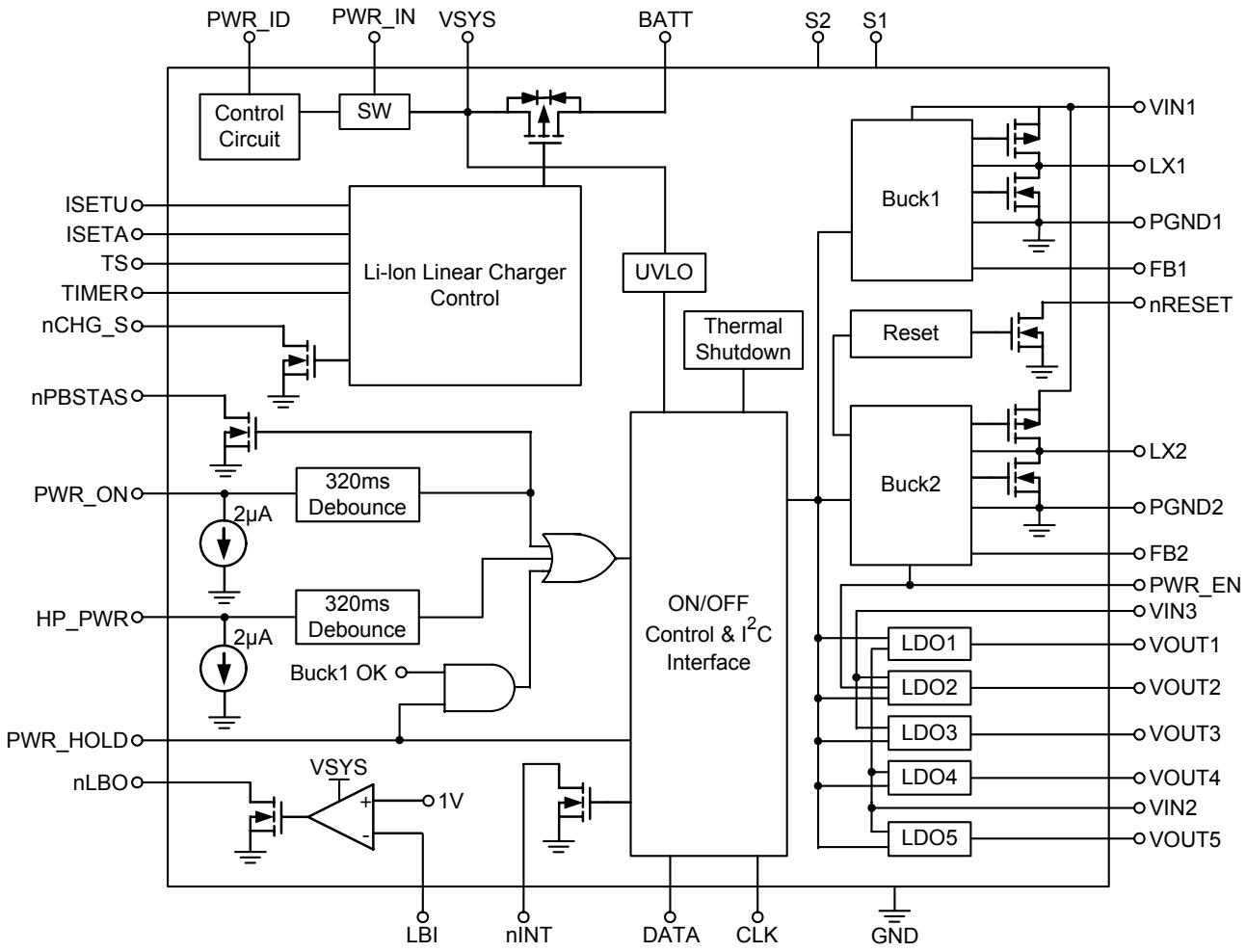
Pin No.	Pin Name	Pin Function
1	nCHG_S	This pin indicates the status of the battery charger. Open Drain Output and Active Low.
2	ISETA	PWR_IN Charge Current Setting Pin.
3	TS	Temperature Sense Pin.
4	TIMER	Charge Time Setting.
5	VOUT2	1.2V/80mA LDO regulator.
6	VIN3	This pin must be shorted to VSYS, VIN1 and VIN2. Connect a 4.7μF ceramic capacitor from VIN3 to GND.
7	VOUT3	1.2V/80mA LDO Regulator with 25mV/Step Adjustable.
8	VOUT1	3.3V/500mA LDO Regulator.
9	VIN2	Must be shorted to VSYS, VIN1 and VIN3. Connect a 10μF ceramic capacitor from VIN2 to GND.
10	VOUT4	2.5V/50mA LDO Regulator.
11	VOUT5	3.3V/50mA LDO Regulator.
12	nPBSTAS	Push-Button Status Pin. This pin is used to inform the power good state to processor. Open Drain Output and Active Low.
13	nRESET	This pin provides a 200ms reset signal during power-up to initialize a processor. Open Drain and Active Low.
14	nINT	This pin must be Active Low to inform processor the interrupt events happened, Open Drain Output and Active Low.
15	nLBO	Low-Battery indication. Open Drain Output and Active Low.
16	LBI	Low-Battery Detection. This pin is used to monitor the VSYS Voltage and the internal reference voltage is 1V
17, 41 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
18	S2	LDO1 & LDO2 Output Voltage Setting, Directly Connect VSYS to Pull High, GND to Pull Low.
19	S1	LDO1 & LDO2 Output Voltage Setting, Directly Connect VSYS to Pull High, GND to Pull Low.
20	PWR_EN	Buck2 & LDO2 Enable Pin from Processor.
21	FB2	Voltage Feedback2. FB2 Regulates to 0.6V nominal.
22	PGND2	Buck 2's Power Ground.
23	LX2	Inductor Connection to the Drains of the Internal N- MOSFETs and P-MOSFETs.
24	VIN1	This pin must be shorted to VSYS, VIN2, and VIN3. Connect a 10μF ceramic capacitor from VIN1 to GND.
25	LX1	Inductor Connection to the Drains of the Internal N-MOSFETs and P-MOSFETs.
26	PGND1	Buck 1's Power Ground.
27	FB1	Voltage Feedback1. FB1 Regulates to 0.6V Nominal.
28,29	BATT	Main Battery Supply Input Terminal. This pin delivers charging current and monitors battery voltage.
30	DATA	Data Input/output for Serial Interface.
31	CLK	Clock Input for Serial Interface.
32	PWR_HOLD	Logic Low Signal from Processor to Turn Off the PMU.

To be continued

Functional Pin Description

Pin No.	Pin Name	Pin Function
33	PWR_ON	Active High Power On / Off Key Input. This pin has an Internal 2μA Pull-Down Current to GND. When the push button is closed, It Is shorted to SYS, not Ground. This input is de-bounced with 320ms (typ).
34	HP_PWR	Logic High Signals Connection of Hands Free Kit. This Pin Has an Internal 2μA Pull-Down Current to GND. This Input is De-bounced with 320ms (typ).
35,36	VSYS	Connect this pin to System with a minimum 22μF ceramic capacitor to GND. This pin must be shorted to VIN1, VIN2, and VIN3
37	PWR_ID	Power Source Input Detection Pin.
38,39	PWR_IN	Power Source Input. Connect a 4.7μF Ceramic Capacitor from this pin to GND.
40	ISETU	USB Charge Current Setting Pin.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- PWR_IN ---------- 0V to 7V
- PWR_HOLD, PWR_ON, HP_PWR, DATA, CLK, nCHG_S, ISETA, TS, TIMER, nPBSTAS, nRESET, nINT, nLBO, LBI, S2, PWR_EN, PWR_ID ---------- –0.3V to VSYS + 0.3V
- FB2, FB1, LX2, LX1 ---------- –0.3V to VIN1 + 0.3V
- VOUT2, VOUT3 ---------- –0.3V to VIN3 + 0.3V
- VOUT1, VOUT4, VOUT5 ---------- –0.3V to VIN2 + 0.3V
- VIN1, VIN2, VIN3 ---------- VSYS–0.3V to VSYS + 0.3V
- BATT, VSYS ---------- 0V to 5.5V
- ISETU ---------- –0.3V to PWR_IN + 0.3V ≤ 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 5x5 ---------- 2.778W
- Package Thermal Resistance (Note 2)
  WQFN-40L 5x5, θ_{JA} ---------- 36°C/W
  WQFN-40L 5x5, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

To be continued

Electrical Characteristics

Electrical Characteristics (General)

(V_{BATT} = 3.7V, $C_{SYS+\Sigma VINx}$ = 47µF, C_{BATT} = 4.7µF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
System Operating Range						
Input Supply Voltage	V_{IN}	Without PWR_IN	3.3	--	5.5	V
Shutdown Supply Current	I_{SHDN}	V_{BATT} = 4.2V, VOUT1 to 5, LX1, LX2 to ground.	4	10	15	µA
Sleep Mode Supply Current		V_{BATT} = 3.7V, PWR_EN = L, Only Buck1, LDO1, LDO3 Turn On	--	120	200	µA
Deep Sleep Mode Supply Current		V_{BATT} = 3.7V	--	100	--	µA
System Voltage Lockout						
Under Voltage Lockout		V_{SYS} Rising	--	3.2	--	V
		V_{SYS} Falling	--	2.5	--	V
Thermal Shutdown						
Threshold			--	160	--	°C
Hystersis			--	10	--	°C
Logic and Control Inputs						
Input Low Level		PWR_HOLD, PWR_ON, HP_PWR, DATA, CLK, PWR_EN, PWR_ID	--	--	0.4	V
Input High Level		PWR_HOLD, PWR_ON, HP_PWR, DATA, CLK, PWR_EN, PWR_ID	1.5	--	--	V
Input Current		PWR_HOLD, DATA, CLK, PWR_EN	–1	--	1	µA
PWR_ON Pull-down Current to GND		PWR_ON = 0.4V	--	2	--	µA
HP_PWR Pull-down Current to GND		HP_PWR = 0.4V	--	2	--	µA
PWR_ON, HP_PWR De-bounce Filter			--	320	--	ms
nINT, nPBSTAS, nRESET, nLBO Pull Down Voltage		Source Current = 5mA	--	65	--	mV

Electrical Characteristics (Buck Converter 1)

(V_{BATT} = 3.7V, $C_{SYS+\Sigma VINx}$ = 47µF, C_{BATT} = 4.7µF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Adjustable Range			0.6		2.5	V
FB Threshold Voltage		V_{FB1} Falling	0.582	0.6	0.618	V
FB1 Threshold Line Regulation		V_{IN} = 2.7V to 5.5V	--	1.5	--	%/V
FB1 Threshold Voltage Hysteresis			--	12	--	mV
Current Limit	I_{LIM}	P-MOSFET Switch	1000	1500	2000	mA
		N-MOSFET Switch	--	700	--	
On-Resistance		P-MOSFET Switch, I_{LX} = –40mA	--	0.3	--	Ω
		N-MOSFET Switch, I_{LX} = 40mA	--	0.38	--	
Rectifier Off Current Threshold			--	30	--	mA

Electrical Characteristics (Buck Converter 2)

(V_{BATT} = 3.7V, $C_{SYS+\Sigma VINx}$ = 47µF, C_{BATT} = 4.7µF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Adjustable Range			V_{REF}	–	2.5	V
Default FB2 Threshold Voltage		V_{FB2} Falling	0.582	0.6	0.618	V
FB2 Threshold Line Regulation		V_{IN} = 2.7V to 5.5V	--	1.5	--	%/V
FB2 Threshold Voltage Hysteresis			--	12	--	mV
Current Limit	I_{LIM}	P-MOSFET Switch	1000	1500	2000	mA
		N-MOSFET Switch	--	700	--	
On-Resistance		P-MOSFET Switch, I_{LX} = –40mA	--	0.4	--	Ω
		N-MOSFET Switch, I_{LX} = 40mA	--	0.4	--	
Rectifier Off Current Threshold			--	30	--	mA
Programmable FB2 Voltage		V_{FB2} Falling	0.5	--	0.7	V
Each Programmable FB2 Voltage Step			--	12.5	--	mV

Electrical Characteristics (VOUT1 (LDO1))

(V_{BATT} = 3.7V, $C_{SYS+\Sigma VINx}$ = 47μF, C_{BATT} = 4.7μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT1}	I_{LOAD} = 200mA & V_{IN} = 3.7V	3.201	3.3	3.399	V
Output Current	I_{OUT}		--	--	200	mA
Current Limit	I_{LIM}	V_{OUT1} = 0V	--	500	850	mA
Dropout Voltage	V_{DROP}	I_{LOAD} = 200mA	--	150	--	mV
Line Regulation		V_{OUT1} + 0.4V ≤ V_{BATT} = V_{IN1} ≤ 5.5V, I_{LOAD} = 200mA	--	2.4	--	mV
Load Regulation		V_{IN1} = 3.7V, 50μA < I_{LOAD} < 200mA	--	25	--	mV
Power Supply Rejection. $\Delta V_{OUT}/\Delta V_{IN}$		F = 10Hz – 10kHz, C_{OUT} = 1μF, V_{OUT} > 2.5V, I_{LOAD} = 30mA	--	60	--	dB

Note : All output capacitors are ceramic and X7R/X5R type.

Electrical Characteristics (VOUT2 (LDO2))

(V_{BATT} = 3.7V, $C_{SYS+\Sigma VINx}$ = 47μF, C_{BATT} = 4.7μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT2}	I_{LOAD} = 80mA & V_{IN} = 3.7V	1.164	1.2	1.236	V
Output Current	I_{OUT}		--	--	80	mA
Current Limit	I_{LIM}	V_{OUT2} = 0V	--	400	--	mA
Line Regulation		V_{OUT2} + 0.4V ≤ V_{BATT} = V_{IN1} ≤ 5.5V, I_{LOAD} = 80mA	--	2.4	--	mV
Load Regulation		V_{IN1} = 3.7V, 50μA < I_{LOAD} < 80mA	--	25	--	mV
Power Supply Rejection. $\Delta V_{OUT}/\Delta V_{IN}$		F = 10Hz – 10kHz ,C_{OUT} = 1μF I_{LOAD} = 30mA	--	60	--	dB

Note : All output capacitors are ceramic and X7R/X5R type.

Electrical Characteristics (VOUT3 (LDO3))

(V_{BATT} = 3.7V, $C_{SYS+\Sigma VINx}$ = 47μF, C_{BATT} = 4.7μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT3}	I_{LOAD} = 80mA & V_{IN} = 3.7 V	1.164	1.2	1.236	V
Output Current	I_{OUT}		--	--	80	mA
Current Limit	I_{LIM}	V_{OUT3} = 0V	--	400	--	mA
Line Regulation		V_{OUT3} + 0.4V ≤ V_{BATT} = V_{IN1} ≤ 5.5V, I_{LOAD} = 80mA	--	2.4	--	mV
Load Regulation		50μA < I_{LOAD} < 80mA	--	25	--	mV
Power Supply Rejection. $\Delta V_{OUT}/\Delta V_{IN}$		F = 1kHz ,C_{OUT} = 1μF I_{LOAD} = 30mA	--	60	--	dB

Note : All output capacitors are ceramic and X7R/X5R type.

Electrical Characteristics (VOUT4 (LDO4))

(V_{BATT} = 3.7V, $C_{SYS+\Sigma VINx}$ = 47μF, C_{BATT} = 4.7μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT4}	I_{LOAD} = 50mA & V_{IN} = 3.7 V	2.425	2.5	2.575	V
Output Current	I_{OUT}		--	--	50	mA
Current Limit	I_{LIM}	V_{OUT4} = 0V	--	400	--	mA
Dropout Voltage	V_{DROP}	I_{LOAD} = 50mA	--	50	--	mV
Line Regulation		V_{OUT4} + 0.4V ≤ V_{BATT} = V_{IN1} ≤ 5.5V, I_{LOAD} = 50mA	--	2.4	--	mV
Load Regulation		50μA < I_{LOAD} < 50mA	--	25	--	mV
Power Supply Rejection. $\Delta V_{OUT}/\Delta V_{IN}$		F = 1kHz , C_{OUT} = 1μF, I_{LOAD} = 30mA	--	60	--	dB

Note : All output capacitors are ceramic and X7R/X5R type.

Electrical Characteristics (VOUT5 (LDO5))

(V_{BATT} = 3.7V, $C_{SYS+\Sigma VINx}$ = 47μF, C_{BATT} = 4.7μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT5}	I_{LOAD} = 50mA & V_{IN} = 3.7 V	3.201	3.3	3.399	V
Output Current	I_{OUT}		--	--	50	mA
Current Limit	I_{LIM}	V_{OUT5} = 0V	--	400	--	mA
Dropout Voltage	V_{DROP}	I_{LOAD} = 50mA	--	50	--	mV
Line Regulation		V_{OUT5} + 0.4V ≤ V_{BATT} = V_{IN1} ≤ 5.5V, I_{LOAD} = 50mA	--	2.4	--	mV
Load Regulation		50μA < I_{LOAD} < 50mA	--	25	--	mV
Power Supply Rejection. $\Delta V_{OUT}/\Delta V_{IN}$		F = 1kHz, C_{OUT} = 1μF, I_{LOAD} = 30mA	--	60	--	dB

Note :All output capacitors are ceramic and X7R/X5R type.

Electrical Characteristics (Li-Ion Charger)

(V_{PWR_IN} = 5V, V_{BATT} = 4V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range and Input Current						
PWR_IN Input Operation Voltage Range			4.5	--	5.5	V
PWR_ID Current			–	--	100	μA
ISETU Pull High Current		I_{SETU} = 0V	–	0.5	–	μA
PWR_IN Standby Current		V_{BATT} = 4.2V	–	300	500	μA
PWR_IN UVP Current		V_{PWR_IN} = 4V, V_{BATT} = 3V	–	150	250	μA
PWR_IN UVP Voltage			–	3.7	–	V
PWR_IN Current Limit		PWR_ID = H, I_{SETU} = H	–	450	500	mA
		PWR_ID = H, I_{SETU} = L	–	--	100	
		PWR_ID = L	–	2300	–	
Voltage Regulation						
BATT Regulation Voltage		I_{BATT} = 60mA	4.158	4.2	4.242	V
System Regulation Voltage			4.8	5	5.2	V
PWR_IN Power FET $R_{DS(ON)}$		I_{AC} = 1A	–	350	–	mΩ
System to Battery $R_{DS(ON)}$			–	--	150	mΩ
PWR_IN to SYS Switch Turn On		$V_{PWR\_IN} - V_{BATT}$	–	150	–	mV
Current Regulation						
ISETA Set Voltage (Fast Charge Phase)		V_{BATT} = 3.5V	–	2.5	–	V
Full Charge Setting Range			100	--	1200	mA
Timer						
TIMER Pin Source Current		V_{TIMER} = 2V	–	1	–	μA
Pre-charge Fault Time		C_{TIMER} = 0.1μF	–	2460	–	s
Charge Fault Time		C_{TIMER} = 0.1μF	–	19700	–	s
Precharge						
BATT Pre-Charge Threshold			–	2.8	–	V
BATT Pre-Charge Threshold Hysteresis			–	100	–	mV
Pre-Charge Current		V_{BATT} < Batt Pre-charge Threshold	–	10	–	%
Recharge Threshold						
BATT Re-Charge Falling Threshold Hysteresis		$V_{REG} - V_{BATT}$	–	100	–	mV
Charge Termination Detection						
Termination Current Ratio (default)		ISETA Pin Voltage	–	250	–	mV
Logic Input/Output						
nCHG_S Pull Down Voltage		I/nCHG_S = 5mA	–	300	–	mV

To be continued

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Protection						
Thermal Regulation			--	125	--	°C
TS Pin Source Current		V_{TS} = 1.5V	94	100	106	μA
TS Pin Low Threshold Voltage			2.45	2.5	2.55	V
TS Pin High Threshold Voltage			0.485	0.5	0.515	V

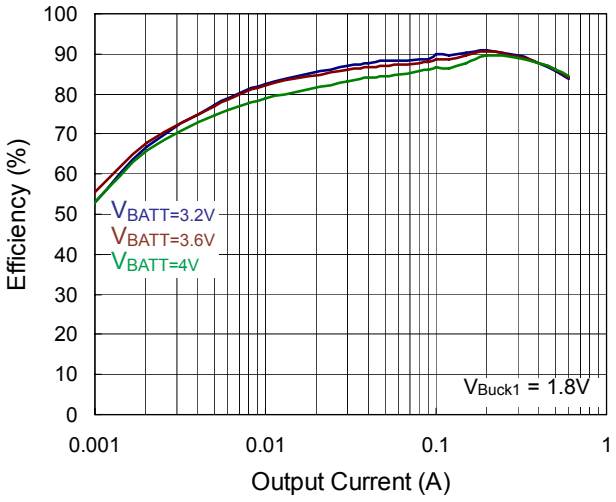
Electrical Characteristics (RESET & Low Battery)

(V_{BATT} = 3.7V, $C_{SYS+\Sigma VINx}$ = 47μF, C_{BATT} = 4.7μF, T_A = 25°C, unless otherwise specified)

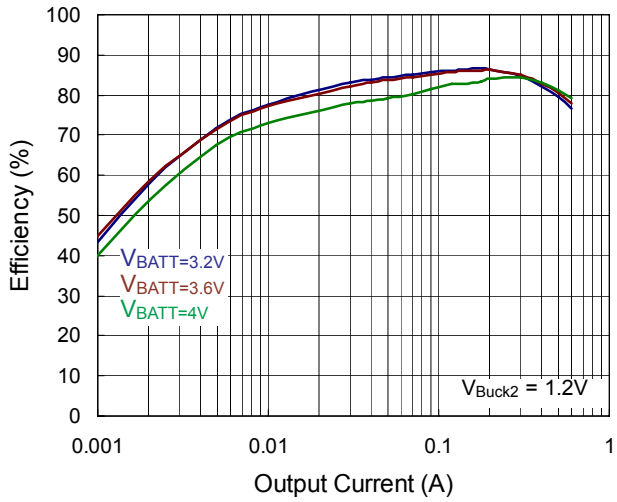
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
nRESET Threshold		With respect to Buck2, Rising	--	87	--	%
nRESET Active Time-out Period		From Buck2 ≥ 87% until RESET = High	--	200	--	ms
LBI Reference Voltage		Falling	--	1	--	V
LBI Hysteresis			--	50	--	mV
LBI Leakage Current			–1	--	1	μA

Typical Operating Characteristics

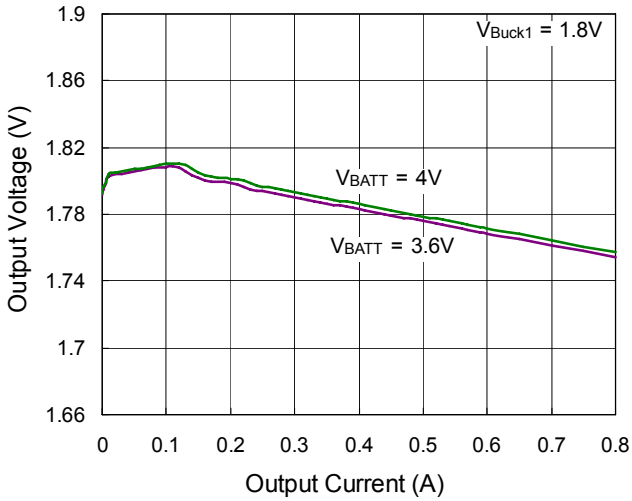
Buck1 Efficiency vs. Output Current



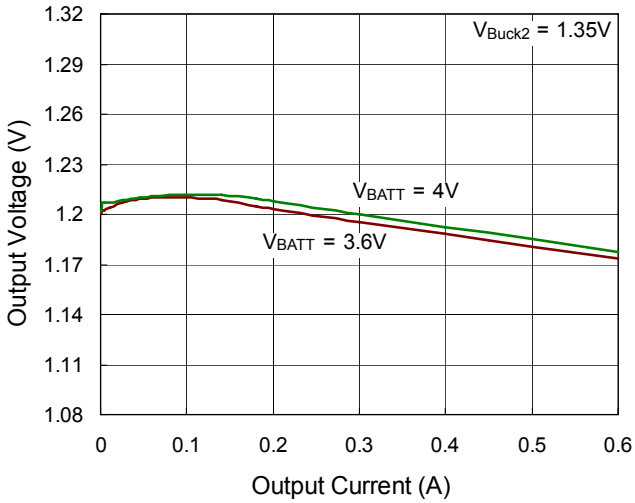
Buck2 Efficiency vs. Output Current



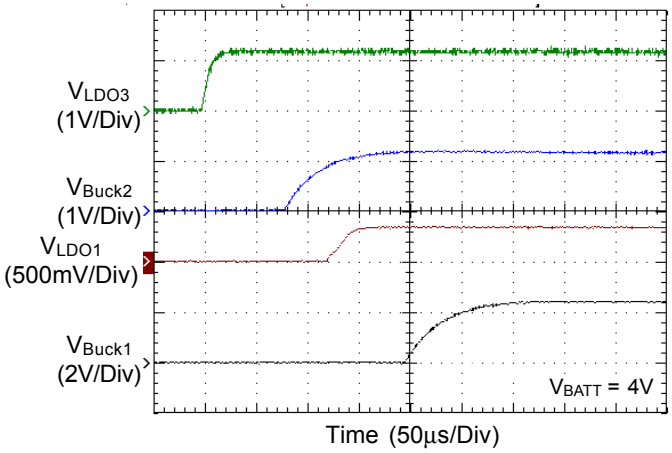
Buck1 Load Regulation



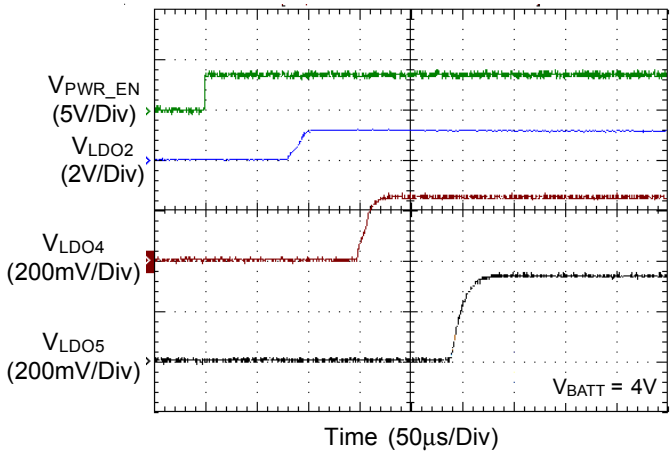
Buck2 Load Regulation



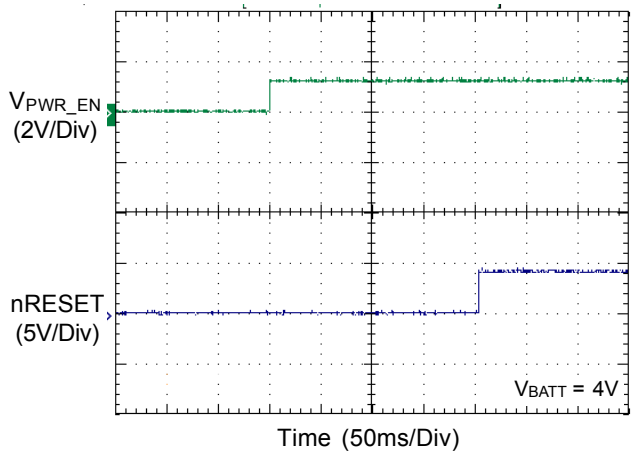
Power On V_{Buck1}, V_{Buck2}, V_{LDO1}, V_{LDO2}



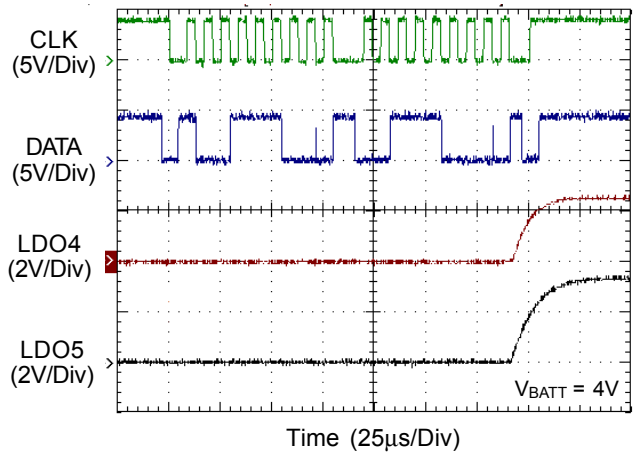
Power On V_{PWR_EN}, V_{LDO2}, V_{LDO4}, V_{LDO5}



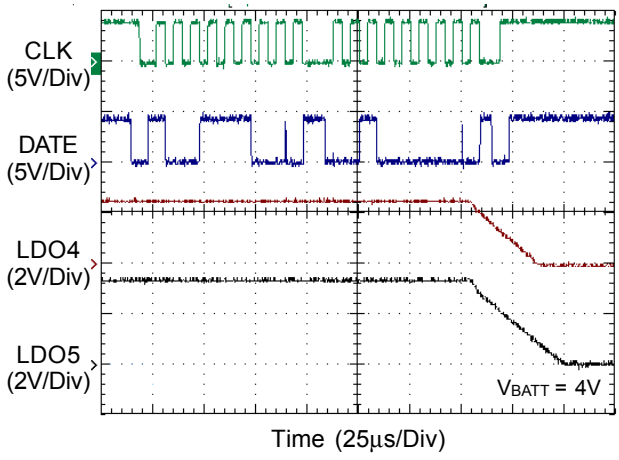
Power On nRESET Response



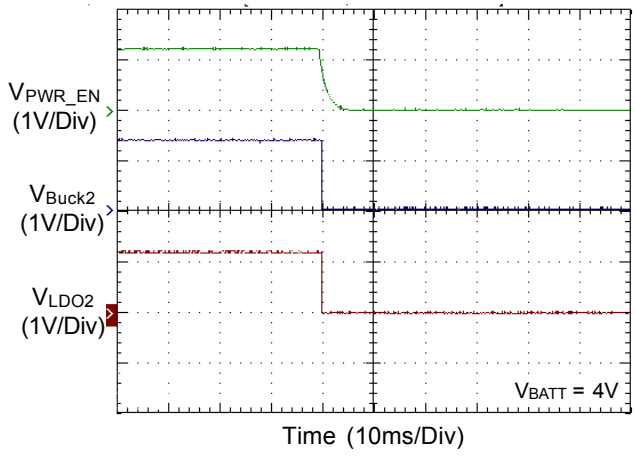
I²C Power On LDO4, LDO5



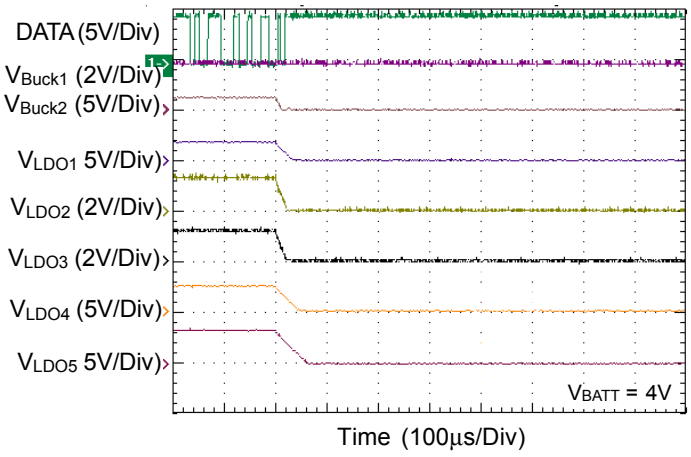
I²C Power Off LDO4, LDO5



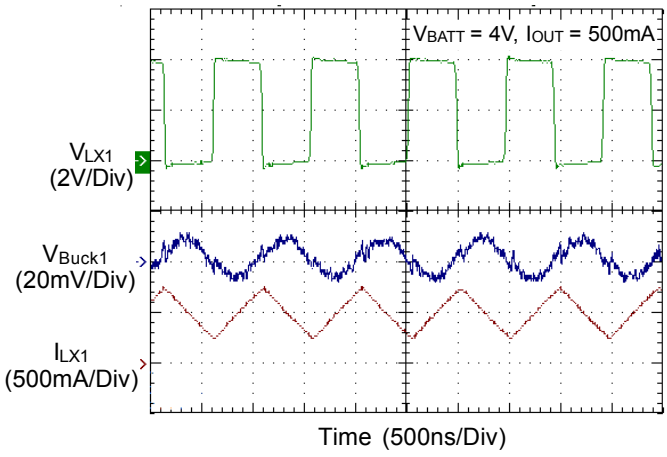
Normal to Sleep Mode



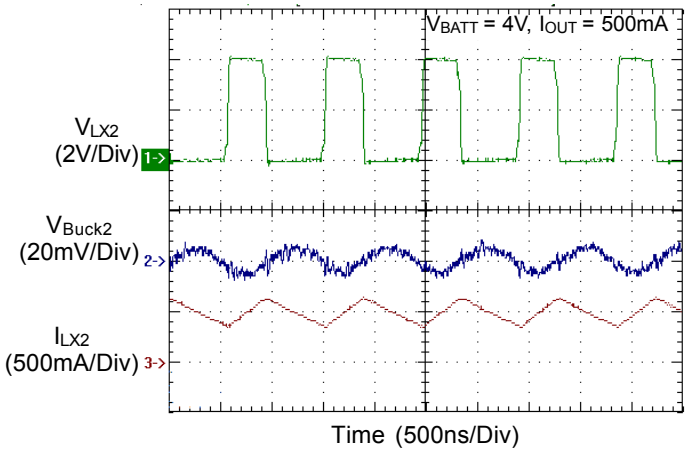
Normal to Deep Sleep Mode



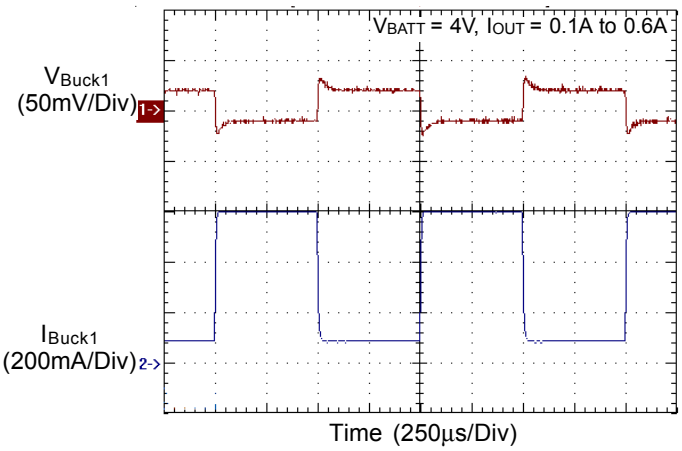
Buck1 Output Voltage Ripple



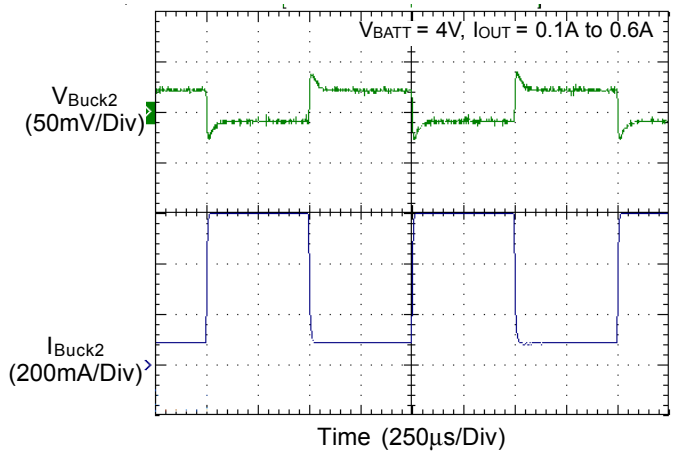
Buck2 Output Voltage Ripple



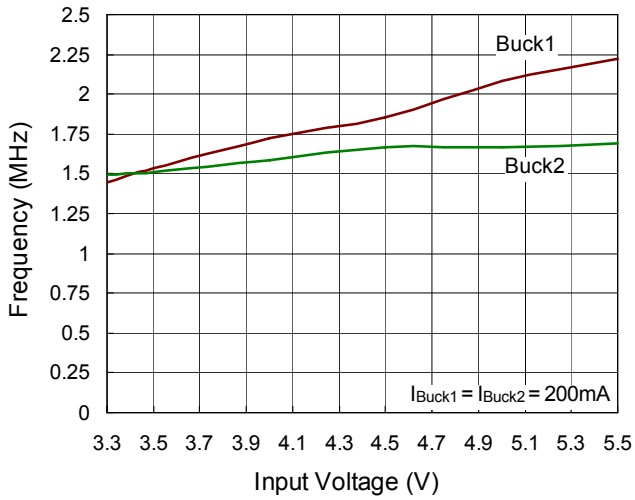
Buck1 Load Transient Response



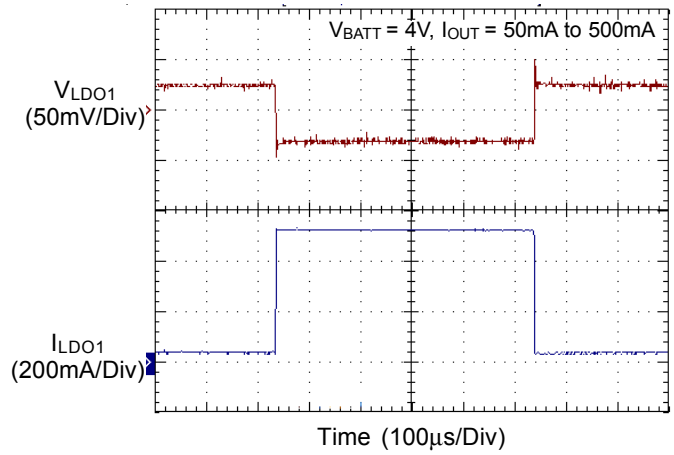
Buck2 Load Transient Response



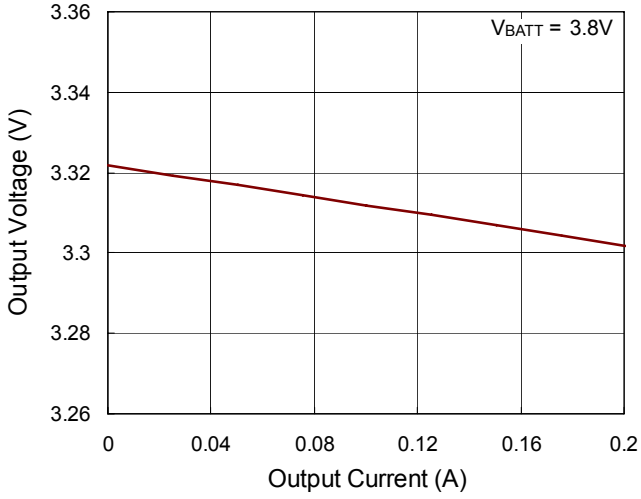
Buck Frequency vs. Input Voltage



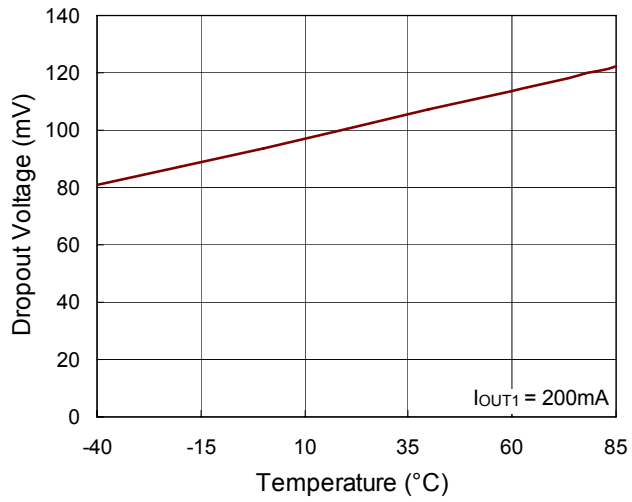
LDO1 Load Transient Response



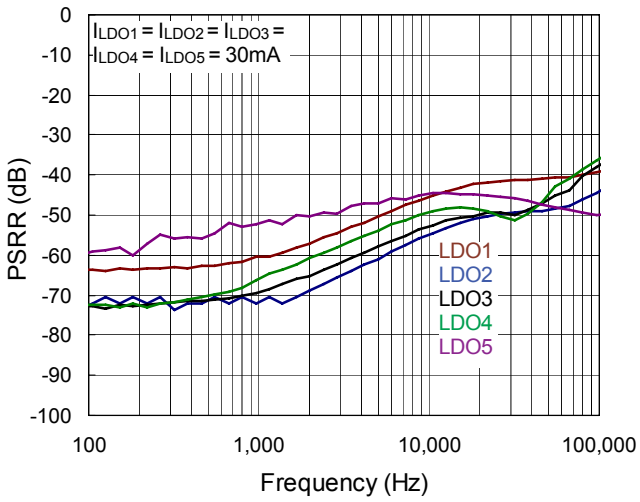
LDO1 Load Regulation



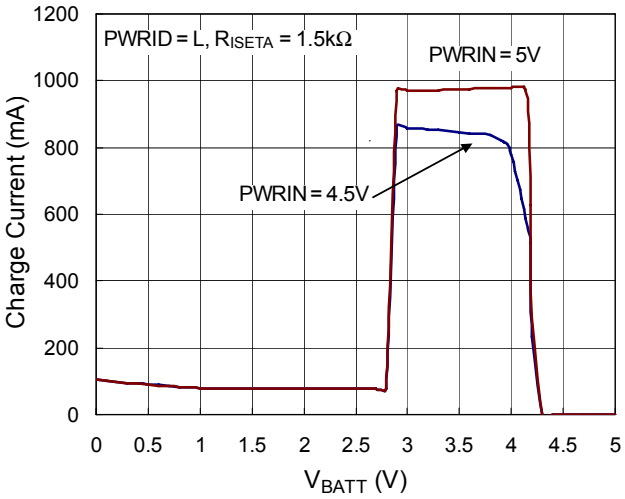
LDO1 Dropout Voltage vs. Temperature



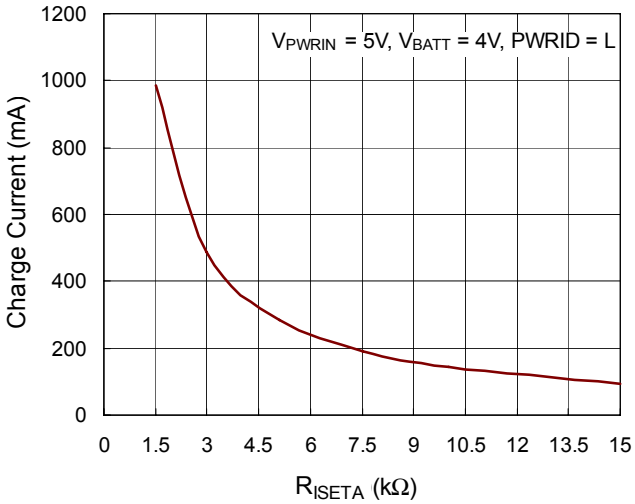
LDO PSRR



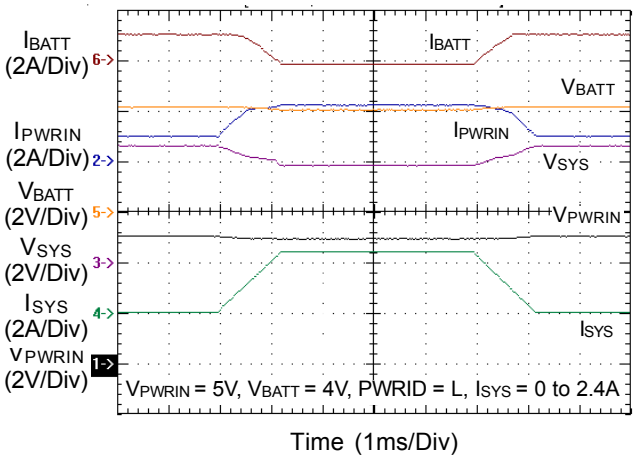
Charge Current vs. BATT Voltage



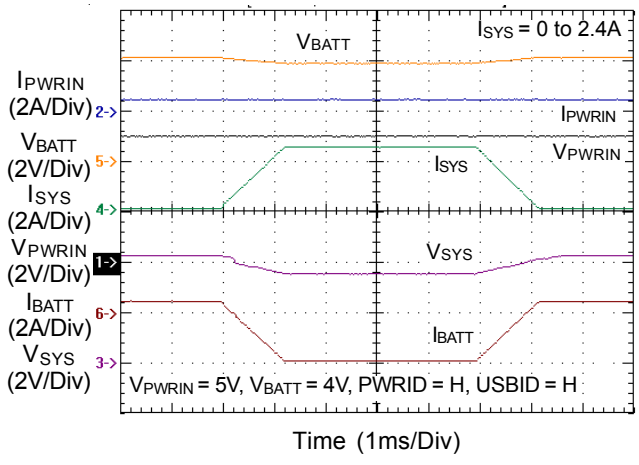
Charge Current vs. R_{ISETA}



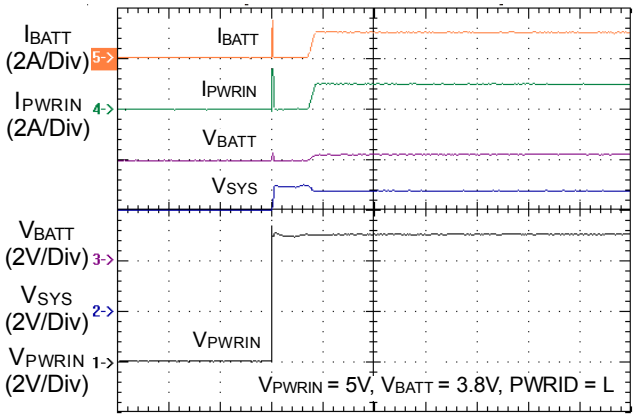
Charger Power Path at AC Mode



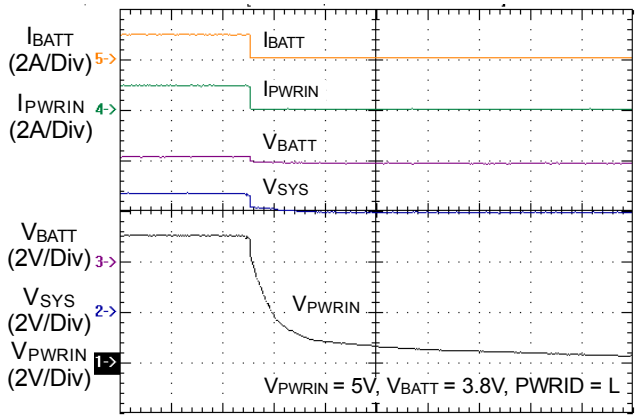
Charger Power Path at USB Mode



PWRIN Insert Response



PWRIN Remove Response



Application Information

I²C Start and Stop Conditions

Both DATA and CLK remain high when the bus is not busy. A high-to-low transition of DATA, while CLK is high is defined as the Start condition. A low-to-high transition of the data line while CLK is high is defined as the Stop condition.

I²C Acknowledge

The number of data bytes between the start and stop conditions for the Transmitter and Receiver are unlimited. Each 8-bit byte is followed by an Acknowledge Bit. The Acknowledge Bit is a high level signal put on DATA by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge after each byte it receives. Also a master receiver must generate an Acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that Acknowledges must pull down the DATA line during the acknowledge clock pulse, so that the DATA line is stable low during the high period of the Acknowledge clock pulse (set-up and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge signal on the last byte that has been clocked out of the slave. In this case, the transmitter must leave DATA high to enable the master to generate a stop condition.

I²C System Configuration

A device on the I²C Bus which generates a "message" is called a "Transmitter" and a device that receives the message is a "Receiver". The device that controls the message is the "Master" and the devices that are controlled by the "Master" are called "Slaves".

I²C Write Command.

The RT9941 writing address set 9C hex and write command and data to set internal register.

TYPE I : Send the address and one command by I²C (Figure 3).

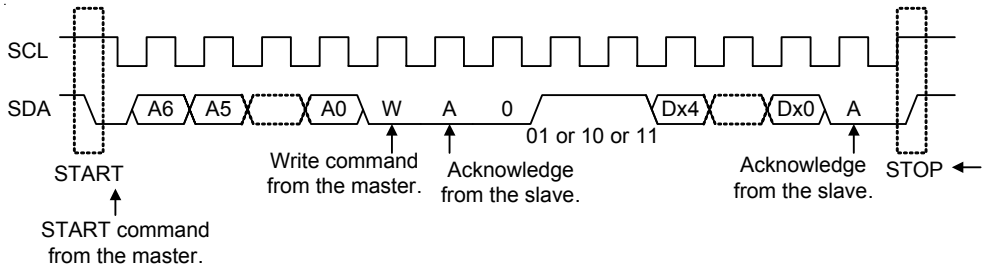


Figure 1. I²C Transmission Flow in the RT9941

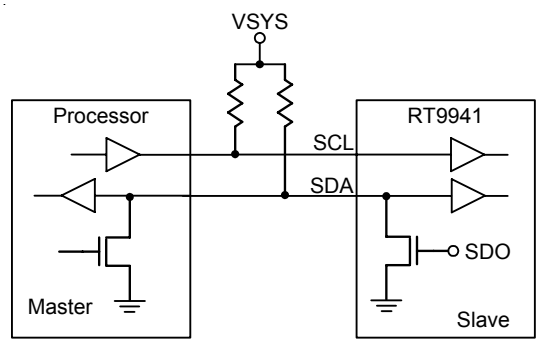


Figure 2. I²C Function Block in the RT9941

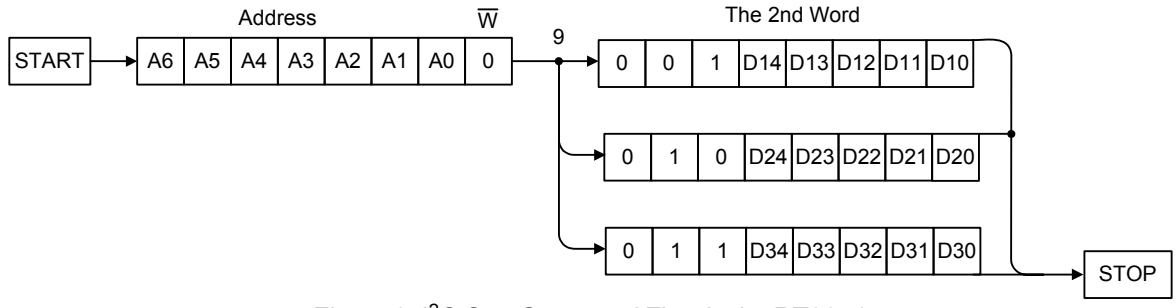


Figure 3. I²C One Command Flow in the RT9941

Table 1. Register Mapping Table (Underline is default)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	0	0	0	0	0	Select Group		
D1	0	0	1	LDO5	LDO4	DS_RDY	PWR_DS[1]	Reserved
				0 / 1	0 / 1	0 / 1	0 / 1	0
				OFF / ON	OFF / ON	None / Deep Sleep Recognition	Power on / Enter to Deep Sleep	
D2	0	1	0	VPROG for LDO5	VPROG for LDO5	VPROG for LDO4	VPROG for LDO4	Charger ON/OFF
				Z51	Z50	Z41	Z40	0 / 1
								OFF / ON
D3	0	1	1	VPROG for Buck2, and LDO3	VPROG for Buck2, and LDO3	VPROG for Buck2, and LDO3	VPROG for Buck2, and LDO3	VPROG for Buck2, and LDO3
				V4	V3	V2	V1	V0

V4	V3	V2	V1	V0	LDO3 Output Voltage (V)	Buck2 FB Voltage (V)
0	0	0	0	0	1.0	0.5
0	0	0	0	1	1.025	0.5125
0	0	0	1	0	1.05	0.525
0	0	0	1	1	1.075	0.5375
0	0	1	0	0	1.1	0.55
0	0	1	0	1	1.125	0.5625
0	0	1	1	0	1.15	0.575
0	0	1	1	1	1.175	0.5875
0	1	0	0	0	1.2 (Default)	0.6 (Default)
0	1	0	0	1	1.225	0.6125
0	1	0	1	0	1.25	0.625
0	1	0	1	1	1.275	0.6375
0	1	1	0	0	1.3	0.65
0	1	1	0	1	1.325	0.6625
0	1	1	1	0	1.35	0.675
0	1	1	1	1	1.375	0.6875
1	X[3]	X	X	X	1.4	0.7

Note a : To enter deep sleep mode, DS_RDY and PWR_DS need to be set.

Note b : If Charger ON/OFF is “0”, the charger will suspend in any external condition until this bit is “1”.

Note c : “X” means don’t care

Z41	Z40	LDO4 Output Voltage (V)
0	0	1.8
0	1	2.5 (Default)
1	0	2.85
1	1	3.3

Z51	Z50	LDO5 Output Voltage (V)
0	0	1.2
0	1	1.5
1	0	3.0
1	1	3.3 (Default)

TYPE II : Send address and two commands by I^2C (Figure 4).

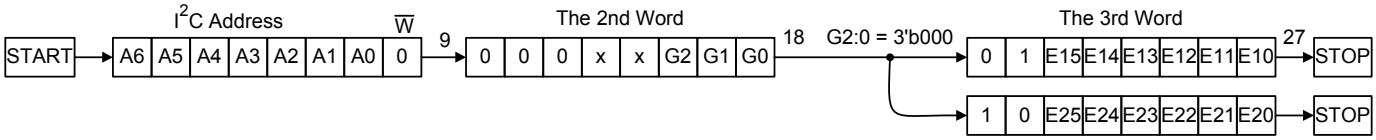


Figure 4. I^2C Two Commands Flow in the RT9941

Group 0 (Bit2 = 0, Bit1 = 0, Bit0 = 0)															
	Bit7	Bit6	Bit5		Bit4		Bit3		Bit2		Bit1		Bit0	
E1	0	1	LDO3		LDO2		LDO1		Buck1		Buck2		PWR_EN	
			0	1	0	1	0	1	0	1	0	1	0	1
			OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	None	Mask
E2	1	0	PWR_IN IN		PWR_IN OUT		PWR_ID		Reserved		TIME OUT		CHG DONE	
			0	1	0	1	0	1	1		0	1	0	1
			None	Mask	None	Mask	None	Mask	(Keep this bit =1)		None	Mask	None	Mask

I²C Read Command.

The RT9941 reading address set 9D hex and read the interrupt status from internal register (Figure 5).

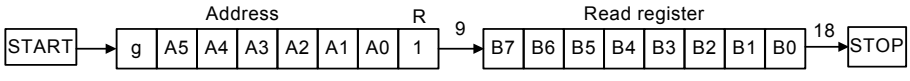


Figure 5. I^2C Read Command of the RT9941

Table 2. The Default Status of Interrupt Registers for I^2C Reading (No PWR_IN)

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PWR_IN	PWR_OUT	PWR_ID	Reserved	Time Out	1	0	PWR_DS
Default	0	1	0	1	0	0	0	0

LDO1 & LDO2 Voltage Setting

Pin S1 and S2 are tri-stat input to set LDO1 and LDO2 voltage. Connect to VSYS directly to pull high and GND to pull low. The Voltage setting table is listed in Table 3.

Table 3. LDO1 & LDO2 Voltage Setting

S1	S2	LDO1 (V)	LDO2 (V)
L	H	3.3	1.2
H	L	2.8	1.2
H	H	2.5	1.2
L	F	1.8	1.2
F	H	2.5	1.3
F	F	1.8	1.3
H	F	3.3	1.3
F	L	2.5	1.0
L	L	3.0	1.2

Power Sequence

If the PWR_IN and VSYS pin voltages are below the internal UVLO threshold, all IC blocks are disabled and the RT9941 is not operational. When an external power source or battery with voltage greater than the UVLO voltage threshold is applied to VSYS pins, the internal RT9941 references are powered up and biasing internal circuits. When all the main internal supply rails are active, the RT9941 I^2C registers are set to the power-up default values.

If a power good fault is not present at the end of the power good check mode and then NORMAL mode starts. In this mode of operation, the I^2C registers define the RT9941 operation, and must be able to handle all issues regarding power on/off the handheld device. The PWR_ON and PWR_HOLD pins determine the power on/off status of the handset.

Logic high on PWR_ON pin is the normal way of powering up a handset. The PWR_ON signal is held high for at least 320 ms; Buck1, 2 and LDO1, 3 are turned on; when Buck2 reaches 87% of its final value, a 200ms reset timer is started at after which nRESET is asserted high, and then the handheld device processor is initialized and will assert PWR_HOLD high to maintain power on. This wrap around constitutes the PWR_ON button can be released (return to low state) and the power remains on. If, however, PWR_ON is released before the PWR_HOLD signal is asserted, then Buck1, 2 and LDO1, 3 will be turned off. All output could be turned off by the processor asserting PWR_HOLD low, if PWR_ON = Low.

The RT9941's default power output voltages for SiRF TitanII and A4 platform are listed in Table 4 as following :

Table 4. The RT9941 for Samsung Platform Power Terminology

	Buck1	Buck2	LDO1	LDO2	LDO3	LDO4	LDO5
Control Pin	PWR_ON	PWR_EN	PWR_ON	PWR_EN	PWR_ON	I^2C	I^2C
Default Output Voltage	1.8V	1.2V Only auto start up in the First time by PWR_ON	3.3V	1.2V	1.2V	2.5V Only auto start up in the First time by PWR_EN	3.3V Only auto start up in the First time by PWR_EN
SiRF Titan II A4	VDDIO_MEM	VDD_PDN	VDDIO VDDIO_PLL	VDD_PLL	VDD_PRE	VDDA2V5_USB, VDDIO_TSC VDDA_TSC, VREF_ADC	VDDA3V3_ USB

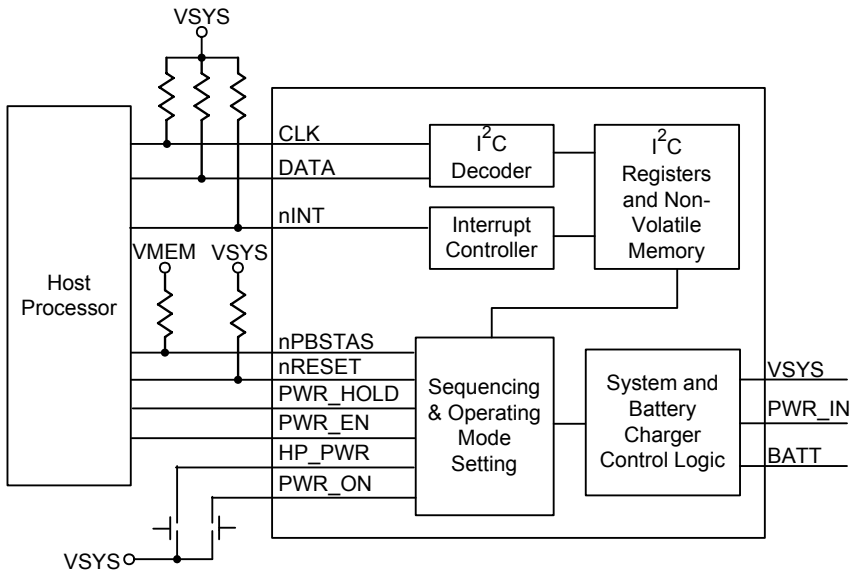


Figure 6. Power and Interface Module

LDO1, 2 voltage setting by Pin S1 and S2

LDO2 and Buck2 can be turned on/off by the external PWR_EN pin.

The I^2C will be activated if the Buck1 is enabled.

LDO 4,5 can be turn on by PWR_EN pin in the first power on sequence.

LDO 1, 2, 3, 4, 5 and Buck1, 2 output voltages can turned on and off by I^2C.

LDO 3, 4, 5 and Buck2 output voltages can be programmed by I^2C.

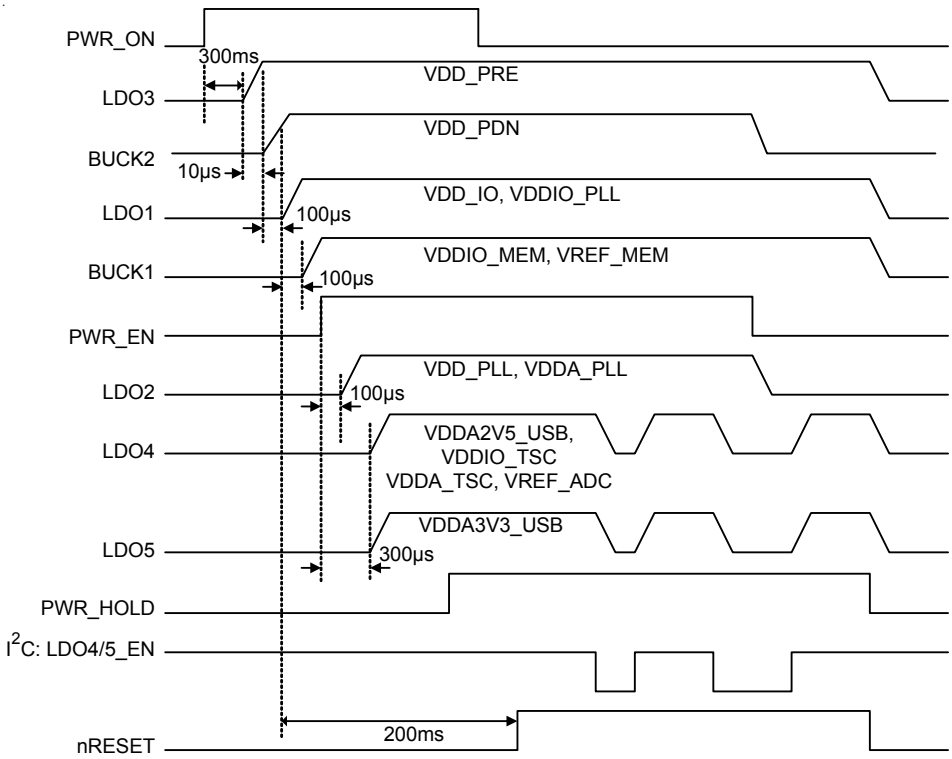


Figure 7. RT9941 POWER ON/OFF Timing Diagram

Sleep Mode

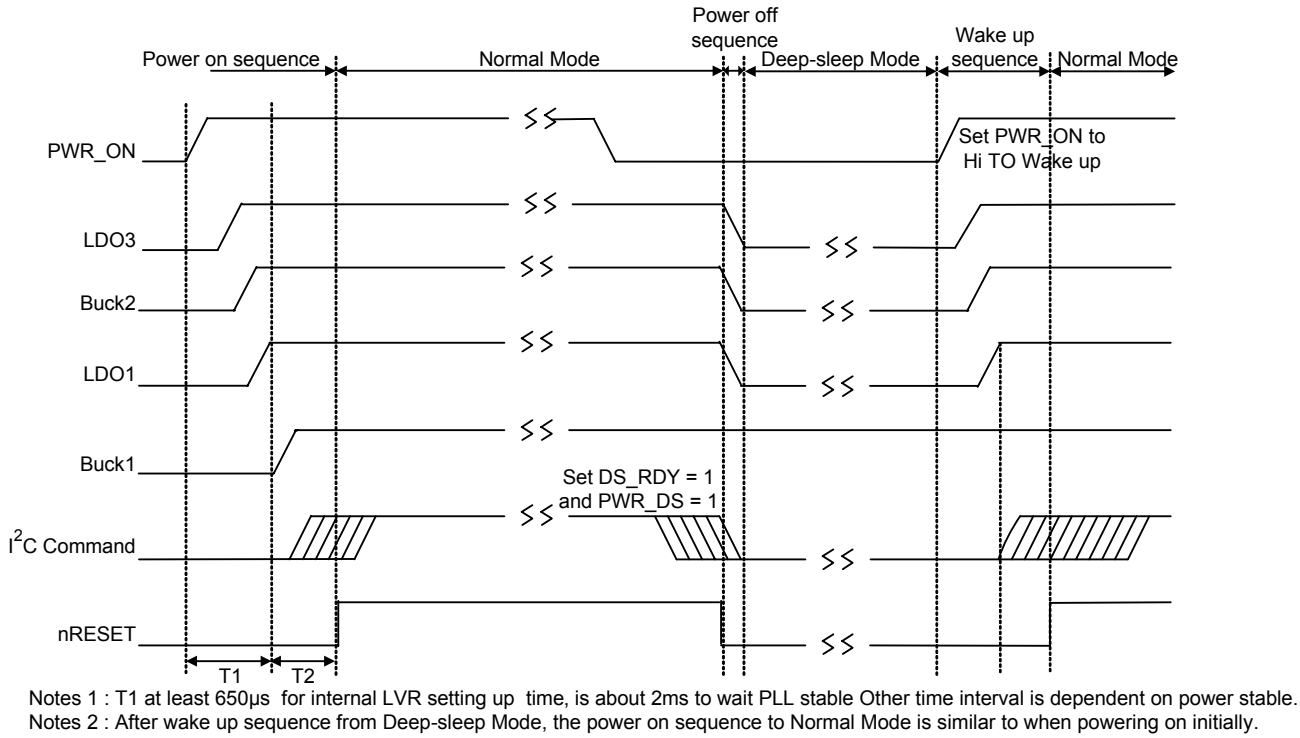
The external host can set the RT9941 in sleep mode using the GPIO configuration. In the sleep mode, change the PWR_EN signal to set different output on/off status :

1. Buck2 and LDO2 will be disabled when the PWR_EN is turned off to enter the sleep mode.

2. When the PWR_EN is turned on, the Buck2 and LDO2 are enabled and the reset signal from the RT9941 remains high.

Deep Sleep Mode

In Deep Sleep Mode, an I^{2}C register is used to control the RT9941 to turn off specific power output. To enter deep sleep mode operation, the RT9941 is needed to set I^{2}C register bits, both DS_RDY = 1 and PWR_DS = 1. After the RT9941 receiving the command by I^{2}C interface , It will just remain Buck1 turn on and all the other power output will be turned off, The RT9941 output reset signal will be driven to low state to processor. If the PWR_ON signal is set to high again, the RT9941 output will be waken up and recovered to the previous state. For recording this deep sleep mode wake up situation, the PWR_DS = 0 and DS_RDY keep high must be made to acknowledge the processor (Figure 8).



Notes 1 : T1 at least 650μs for internal LVR setting up time, is about 2ms to wait PLL stable Other time interval is dependent on power stable.
Notes 2 : After wake up sequence from Deep-sleep Mode, the power on sequence to Normal Mode is similar to when powering on initially.

Figure 8. RT9941 Deep Sleep Mode Timing Diagram

The relationship between I^{2}C register and different mode setting is listed in Table 5.

Table 5. Different mode setting by PWR_DS and DS_RDY

System Mode	PWR_DS	DS_RDY
Normal Mode (Default Status)	0	0
To Enter Deep Sleep Mode	1	1
Power on From Deep Sleep Mode	0	1

Interrupt Mode

The RT9941 interruption controller monitors multiple system status parameters and signals to the host when one of the monitored parameters toggled, as a result of system status change. If the external interrupt event happened, the internal interrupt flag of the RT9941 will be triggered. The interrupt flag with no mask will set the nINT to low state. The host processor receivers the active low signal and then try to read the interrupt register by I^2C interface. The interrupt controller setting and function in register are listed in the Table 6.

Table 6. Interrupt Register Table

Register	Name	Default	Function	INT Event
Bit7	PWR_IN	0	If PWR_IN = Hi, this bit will be set.	Yes
Bit6	PWR_OUT	1	If PWR_IN= Lo, this bit will be set.	Yes
Bit5	PWR_ID	0	If PWR_IN =H &PWR_ID=H This bit will be set.	Yes
Bit4	Reserved	1		No
Bit3	TIME_OUT	0	This bit will be set if time out.	Yes
Bit2	CHG_DONE	0	This bit will be set if charge done.	Yes
Bit1	DS_RDY	0	If PMU enter to deep sleep mode, this bit will be set.	No
Bit0	PWR_DS	0	If PMU power on from deep sleep mode, this bit need to be set.	No

If this internal interrupt event is set without mask, the interrupt controller will set nINT to low if any interrupt behavior happened. Then processor will be acknowledged by nINT and then read register status by I^2C interface. PMU will accept this READ OK status and let the nINT return to high (Figure 9). If this internal interrupt register is set with mask, the interrupt controller will not set nINT to low even external real interrupt event happened (Figure 10).

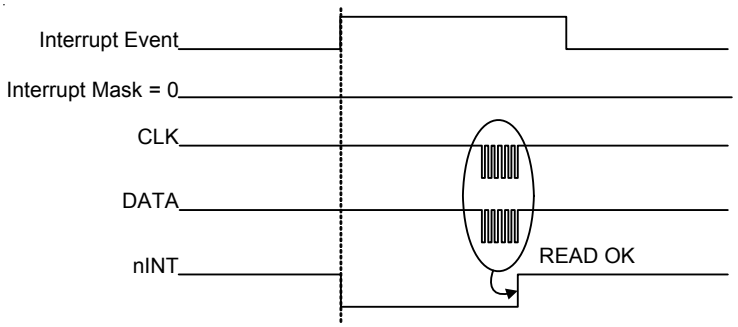


Figure 9. Interrupt without Mask

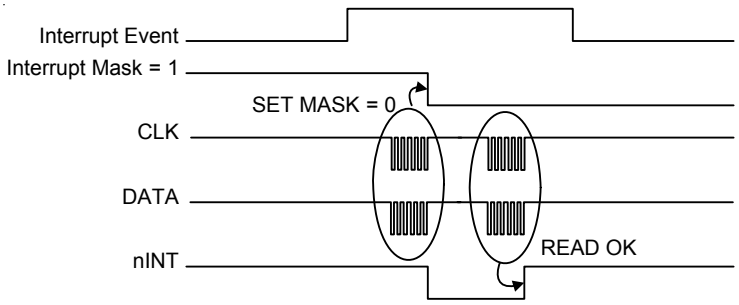


Figure 10. Interrupt with Mask

PWR_ON & HP_PWR & nPBSTAS

Connecting external signal such as head phone can start up the power sequence of power management circuit. When the RT9941 detects a HP_PWR rising edge signal and generates a over 320ms pulse. All RT9941 output will be turned on even the without recognizing PWR_ON signal. The handheld device processor is initialized and will assert PWR_HOLD to high to maintain the RT9941 power remains on. This power on behavior is same as PWR_ON signal asserted. nPBSTAS signal is an inverter of PWR_ON with 320ms de-bounced to inform SOC or uP that power on button has been pressed. PWR_ON & HP_PWR & nPBSTAS timing control diagram in the Figure 11.

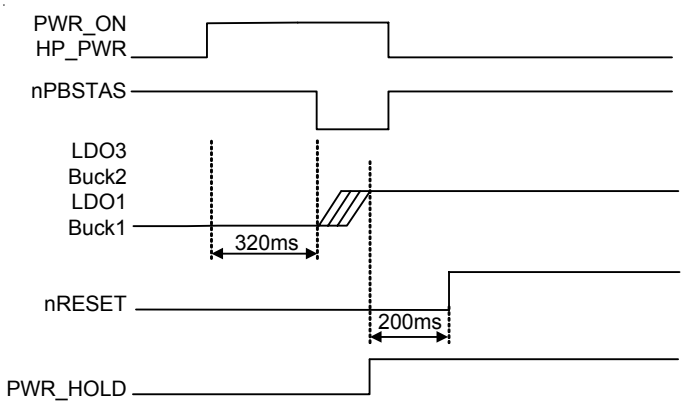


Figure 11. PWR_ON & HP_PWR & nPBSTAS Timing Diagram

Buck Converters

The RT9941 step-down converters are optimized for high efficiency over a wide load range, small external component size, low output ripple, and excellent transient response. The DC/DC converters also feature an optimized on-resistance internal MOSFET switch and synchronous rectifier to maximize the efficiency and minimize the external components. The RT9941 utilizes a proprietary hysteretic PWM control scheme that switches with nearly fixed frequency, allowing the customer to trade some efficiency for smaller external component, as desired. If one buck converter is not used, please make LX = open, FB = IN, and PGND = GND.

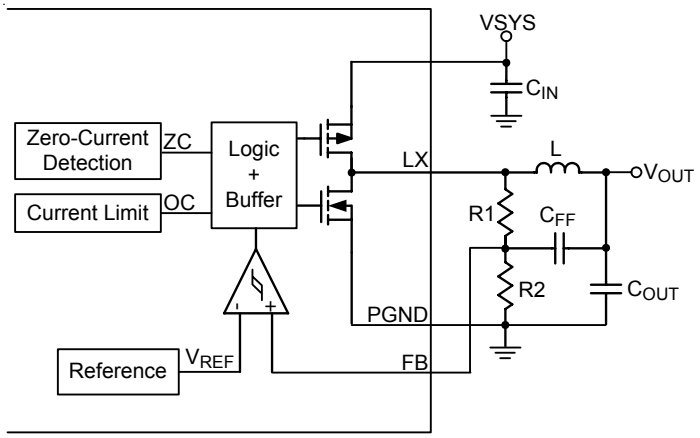


Figure 12. Step-down Converter Block Diagram

Setting the Output Voltage

Select an output voltage between 0.6V and 2.5V by connecting FB to a resistive voltage divider between LX and GND. Choose R2 for a reasonable bias current in the resistive divider. A wide range of resistor values is acceptable, but a good starting point is to choose R2 as 100kΩ. Then, R1 is given by :

$V_{OUT} = \left(\frac{R1}{R2} + 1\right) \times V_{FB1}$, where V_{FB1} is the feedback reference voltage (0.6V typ.)

Below table is the default value of resistor and C_{FF} for different output voltages.

V_{Buck} (V)	R1 (k)	R2 (k)	C_{FF} (pF)
1.2	100	100	220
1.8	200	100	120
2.5	316	100	120

Inductor Selection

The RT9941 step-down converters operate with inductors of 1μH to 4.7μH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor's DC current rating only needs to match the maximum load current of the application because the RT9941 step-down converters feature zero current overshoot during startup and load transients. The recommended inductor is 2.2μH. For optimum voltage positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. For higher efficiency at heavy loads (above 200mA) or minimal load regulation (but some transient overshoot), the resistance should be kept below 100mΩ. For light load applications up to 200mA, much higher resistance is acceptable with very little impact on performance.

Output Capacitor Selection

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and to ensure the regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their characteristics of small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. For most applications, a 4.7μF capacitor is sufficient.

Feedforward Capacitor Selection

The feedforward capacitor, C_{FF}, sets the feedback loop response, controls the switching frequency, and is critical in obtaining the best efficiency possible. Choose a small ceramic X7R capacitor with value given by :

$C_{FF} = \frac{L}{R1} \times 10$

Select the closest standard value to C_{FF} as possible.

Charger

The RT9941 has an integrated charger with power path integrated MOSFETs. This topology, shown in the simplified block diagram (Figure 13), enables the goal of using an external input power to run the system and charge the battery. The power path has single inputs that can be used to select either an external AC_DC adapter or USB port by PWR_ID pin and different charging current by limitation. The RT9941 connects the end equipment main power rail and charges the battery pack by the BATT pin.

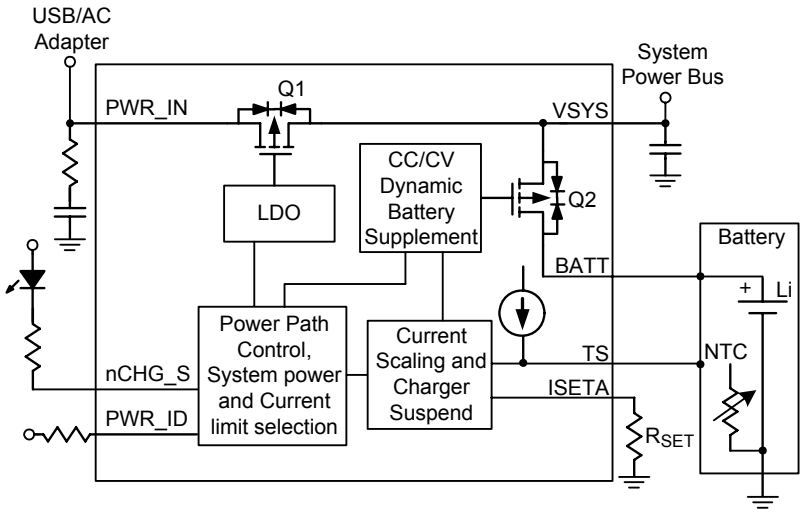


Figure 13. Charger Block Diagram and Required External Components

The RT9941 charger uses current, voltage, and thermal control loops to charge and protect a single Li+ battery cell. One enable input PWR_ID pin is supplied to set charging current limits. During pre-charge and fast-charge phases, the charger output status is pulled low. As the battery voltage approaches 4.2V, the charging current is reduced. When the charging current drops below 10% of charging current setting and the battery voltage equals 4.2V, the nCHG_S output pin goes high impedance, signaling a full battery and set the internal I^2C register bit CHG DONE. If the charger done is not masked, the interrupt flag will be trigged. At any time during charging, if the RT9941 internal I^2C register bit, Charger ON/OFF, is clear. Then the charger enters suspend mode, charging stops, and nCHG_S goes high impedance.

Battery Charge Management Function

The RT9941 supports charging of single-cell Li-Ion battery packs. The charge process is executed in three phases: pre-charge (or preconditioning), constant current and constant voltage. A typical charge profile and flow chart are shown in Figure 14 & 15.

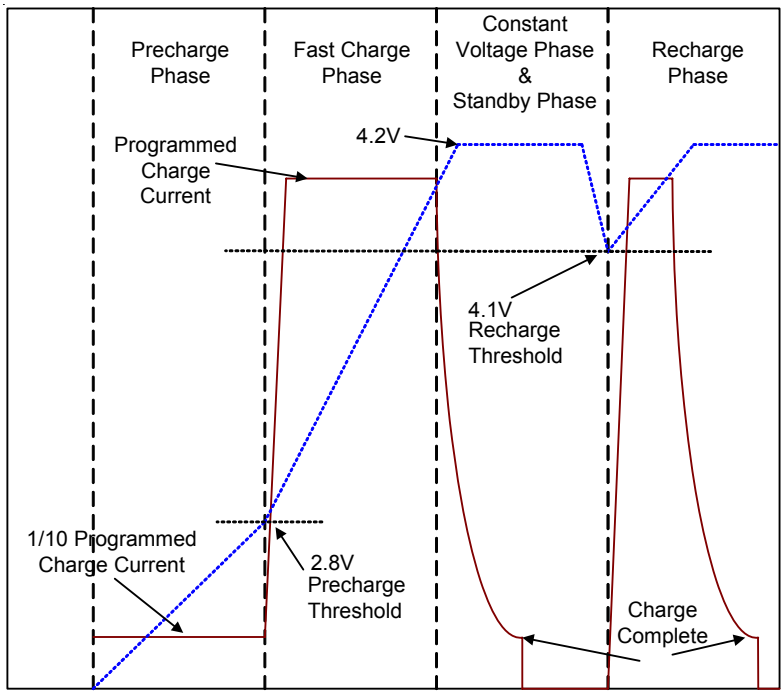


Figure 14. Typical Charge Profile

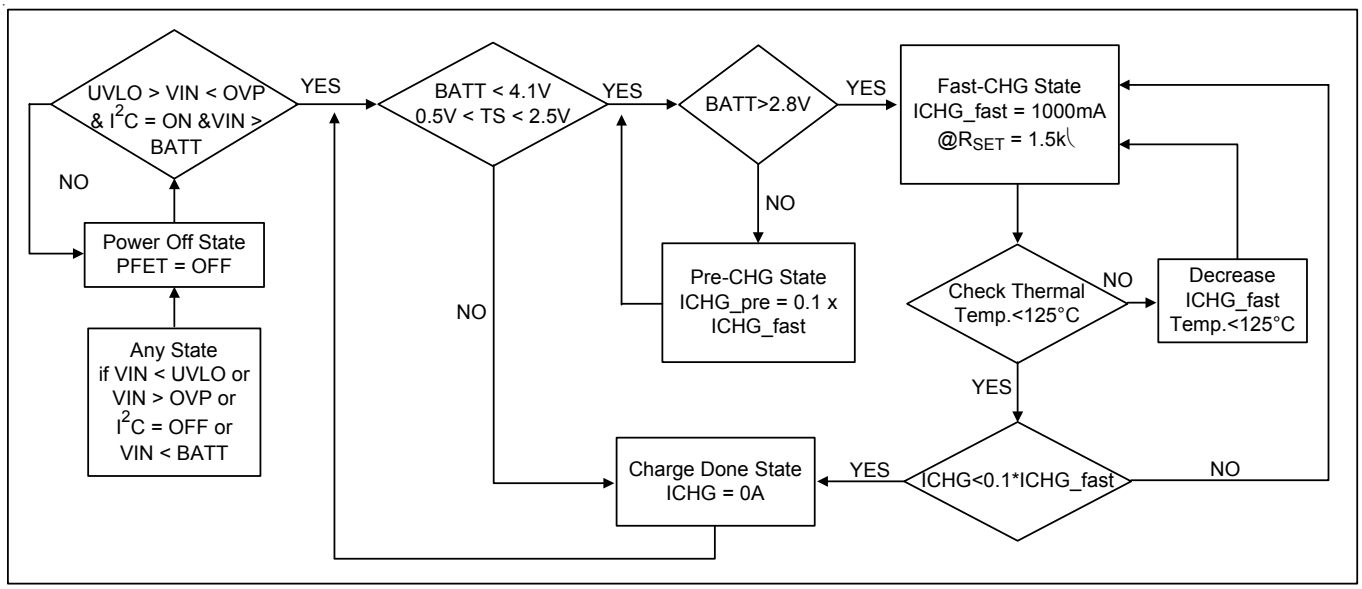


Figure 15. Charge Flow Chat

Power-Path Management

The power path and charge management block operate independently of the other RT9941 circuits. Internal circuits check battery parameters (pack temperature, battery voltage and charge current) and system parameters, setting the power path MOSFETs operating modes automatically. The RT9941 has integrated comparators that monitor the battery voltage, Power input pin voltage and the SYS pin voltage. The data generated by those comparators is used by the power path control logic to define which of the integrated power path switches is active.

A typical auto power path management profile is shown in Figure 16 & 17.

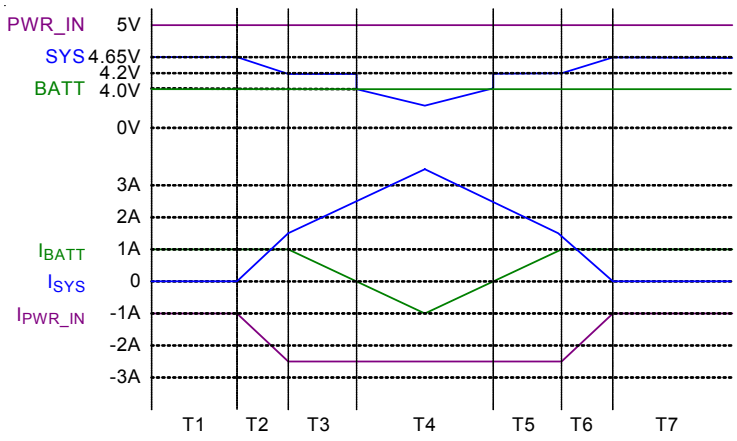


Figure 16. Typical Power Path Management Profile

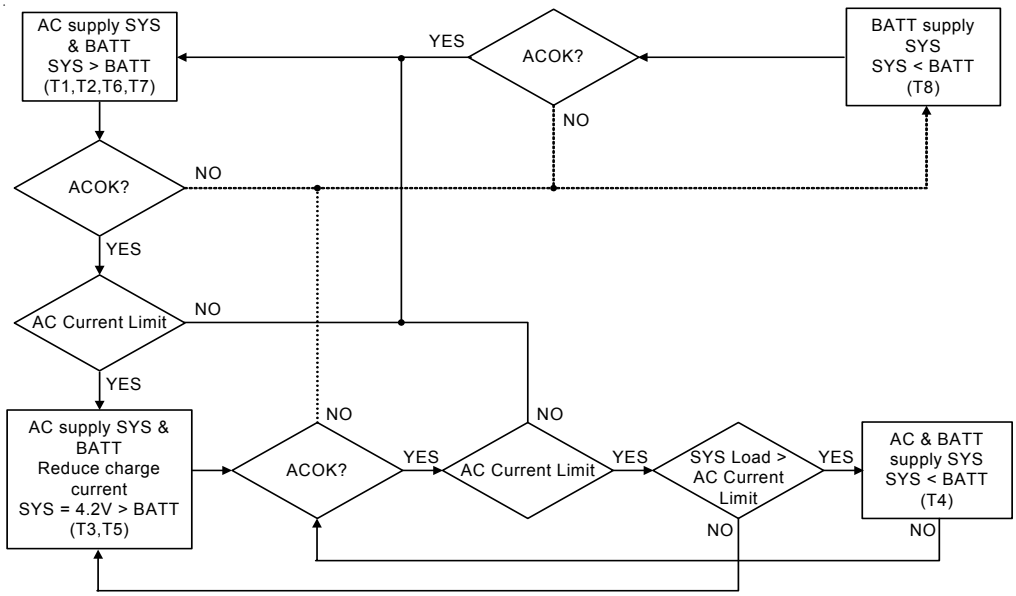


Figure 17. Power Path Management Flow Chart

The RT9941 powers the system while independently charging the battery. This feature reduces the charge and discharge cycles on the battery, allows for proper charge termination, and allows the system to run with an absent or defective battery pack. This feature gives the system priority on input power, allowing the system to power up with a deeply discharged battery pack. This feature works as follows:

Case 1: AC Mode (PWR_ID = LOW)

In this case, the system load is powered directly from the AC adapter through the internal transistor Q1 (Figure 18). The output SYS is regulated at 5.0 V. If the system load exceeds the capacity of the supply, the output voltage drops down to the battery's voltage.

When in AC mode, the battery is charged through the switch Q2 based on the charge rate set on the ISETA input pin. This feature monitors the output voltage (system voltage) for input power loss due to brown outs, current limiting, or removal of the input supply. If the voltage on the VSYS pin drops to a preset value(4.2V) due to a limited amount of input current, then the battery charging current is reduced until the VSYS stops dropping. If the system continues increasing load to exceed the AC adapter capacity, the battery will start to discharge to VSYS.

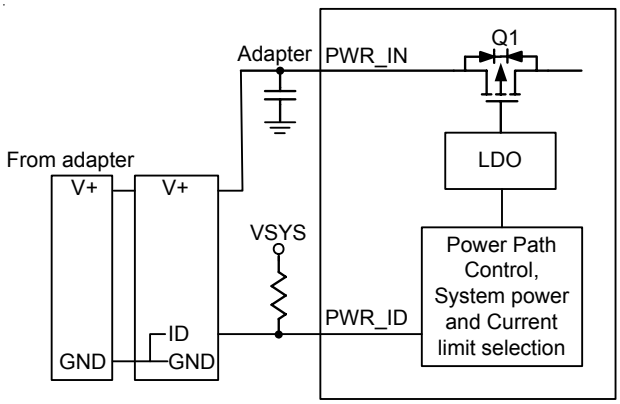


Figure 18. RT9941 Powered by AC Adapter

Case 2: USB Mode (PWR_ID = High)

In this case, the system load is powered from a USB port through the internal switch Q1 (Figure 19). Note that in this case, Q1 regulates the total current to the 450mA level as selected on the input. The output, SYS, is regulated to 5V. The system's power management is responsible for keeping its system load below the USB current. Otherwise, the output drops (VSYS) to the battery voltage; therefore, the system should have a low-power mode for USB power application.

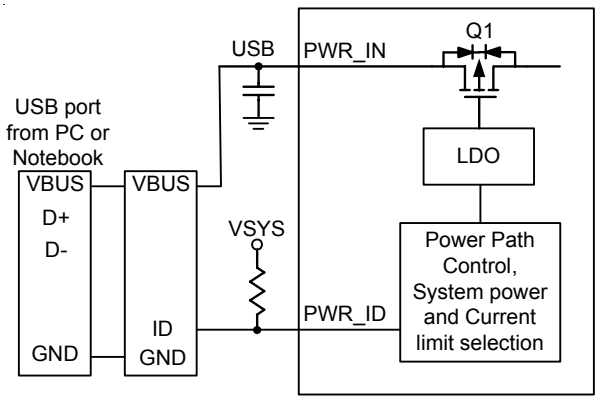


Figure 19. RT9941 Powered byUSB Port

Table 7. PWR_IN Input Current and Charger Current-Limit Selection

PWR_ID	PWR_IN Current Limit	Expected Input Type	Charger Current Limit
Hi	450mA	USB	450mA
Lo	2.3A	AC adapter	(2.5V/Rset)*600

Charge-Current Selection

When powered from a USB port, the input current is available to 0.5 A. For AC-Adapter input applications (PWR_ID = Low) requiring a different current requirement, set the charging current with an external resistor (R_{SET}) from ISETA to GND. Calculate charge current as follows :

Charge Current = 2.5/ R_{SET}(kΩ) x 600 (mA)

The RT9941 offers ISETA pin to determine the AC charge rate from 100mA to 1A.

Charge-Status Output

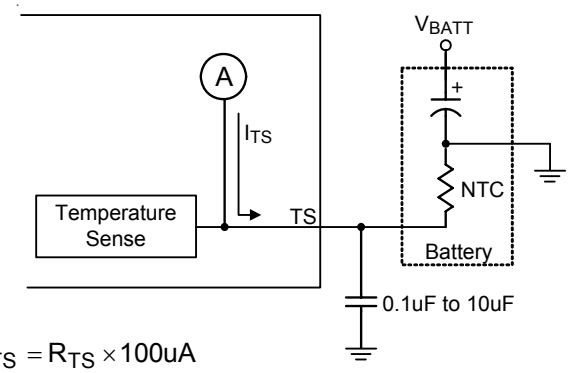
nCHG_S is an open-drain output that indicates charger status and can be used with an external LED. nCHG_S goes low during charging. When VBAT equals 4.2V and the charging current drops below 10% of the setting charge current, nCHG_S goes high impedance and the RT9941 internal I^2C register bit CHG DONE will be set. Connect a pull-up resistor between nCHG_S and VSYS to indicate charge status.

Soft-Start

To prevent input transients, the change rate of the charge current is limited when the charger is turned on or changes its current compliance. It takes approximately 1ms for the charger to go from 0mA to the maximum fast-charge current.

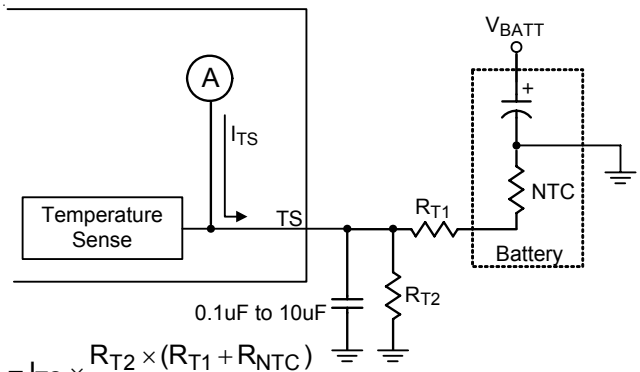
Temperature Monitoring

The RT9941 monitors the battery temperature by measuring the voltage between the TS and GND pins. The RT9941 has an internal current source to provide the bias for most common 10kΩ negative-temperature thermistor (NTC) with the battery.



$$V_{TS} = R_{TS} \times 100uA$$

Figure 20. Connection of Battery Temperature Monitor



$$V_{TS} = I_{TS} \times \frac{R_{T2} \times (R_{T1} + R_{NTC})}{R_{T1} + R_{T2} + R_{NTC}}$$

Figure 21. Connection of Battery Temperature Monitor With Divider

The RT9941 compares the voltage on the TS pin against the internal V_{TS} thresholds to determine if charging is allowed. When the temperature outside the V_{TS} thresholds is detected, the device immediately stops the charger. Charging is resumed when the V_{TS} is recovered to the operation range. However, the user may modify thresholds by adding external resistors to change biasing voltage.

Timer

As a safety mechanism, the charger has a user programmable timer that monitors the pre-charge and fast charge time. This timer (charge safety timer) is started at the beginning of the pre-charge and fast charge period. The safety charge timeout value is set by the value of an external capacitor connected to the TIMR pin (C_{TIMR}), if pin TIMR is short to GND, the charge safety timer is disabled.

As C_{TIMR} = 0.1μF, T_{FAULT} is C_{TIMR} (F) x 1.97 x 10^{11} secs = 19700 secs and $T_{PRECH} = T_{FAULT}$ /8

As timer fault, re-plug-in power or I^2C ON/OFF charger again can release the fault condition.

SYS Output

The RT9941 contains a SYS output which can be regulated up to 5V. Bypass SYS to GND with a 22μF or larger ceramic capacitor to improve the transient droops. When charging a battery, the load on SYS is serviced first and the remaining available current goes to charge the battery.

Battery PRE-CHARGE

During a charge cycle, if the battery voltage is below the V_{PRECH} threshold and the RT9941 applies a pre-charge mode to the battery. This feature revives deeply discharged cells and protects battery life. The RT9941 internally determines the pre-charge rate as 10% of the fast charge current.

Thermal Regulation

The RT9941 features a thermal limit that reduces the charge current when the die temperature exceeds +125°C. As the temperature increases, the RT9941 features a junction temperature regulation loop. If the power dissipation of the IC results in a junction temperature greater than the thermal regulation threshold (125°C), the RT9941 throttles back on the charge current in order to maintain a junction temperature around the thermal regulation threshold (125°C). The RT9941 monitors the junction temperature, T_J, of the die and disconnects the battery from the input if T_J exceeds 125°C. This operation continues until junction temperature falls below the thermal regulation threshold (125°C) by the hysteresis level. This feature prevents the maximum power dissipation from exceeding typical design conditions.

Capacitor Selection

Connect a ceramic capacitor from PWR_IN to GND as close to the IC as possible for proper stability. For most applications, connect a 4.7μF ceramic capacitor from IN to GND as close to the IC as possible.

Linear Regulators

The RT9941 offers five Integrated Linear Regulators, designed to be stable over the operating load range with the use of external ceramic capacitors.

All the LDO have an ON/OFF control which can be set by I2C commands and have integrated switches that discharge each output to ground when the LDO is turned off. The LDO 1, 3 will be turn on in the first time of PWR_ON button be pressed and LDO2 will be turned on when PWR_EN = 1. LDO 4, 5 need to be turned on/off by I^2C command. The LDO4,5 also support four voltage setting by I2C control. LDO1 and LDO2 voltages are set by the S1, S2 pin, see Table 3.

Low-Battery Detector

nLBO is an open-drain output that typically connects to the BATT FAULT input of the processor to indicate the battery has been removed or discharged. nLBO is typically pulled up to VSYS. LBI monitors the input voltage (usually connect to VSYS) and triggers the nLBO output (Figure 22). nLBO is high impedance when the voltage from LBI exceeds the battery rising threshold VLBITH =1.05V (typ.). nLBO is low when the voltage from LBI falls below the low-battery falling threshold VLBITH =1V (typ) (Figure 23). Connecting LBI to two-resistor voltage divider to detect the external resistor embedded in a battery pack and is also used as a pack ID function. When system first power up or back from deep sleep mode , LBI will check the VSYS voltage. If VSYS voltage is lower than setting voltage, system will not power up or wake up. If the low-battery-detector feature is not required, connect nLBO to ground and connect LBI to SYS.

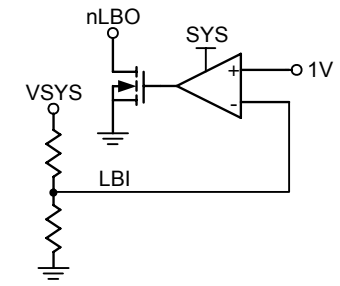


Figure 22. LBI and nLBO Application Circuit

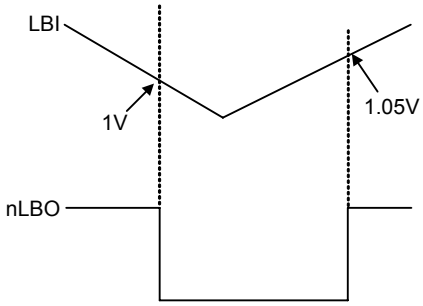


Figure 23. Typical LBI Rising and Falling Threshold Voltage.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9941, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-40L 5x5 packages, the thermal resistance θ_{JA} is 36° C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C - 25°C) / (36°C/W) = 2.778W for WQFN-40L 5x5 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J\ (MAX)}$ and thermal resistance θ_{JA}. For RT9941 packages, the Figure 24 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

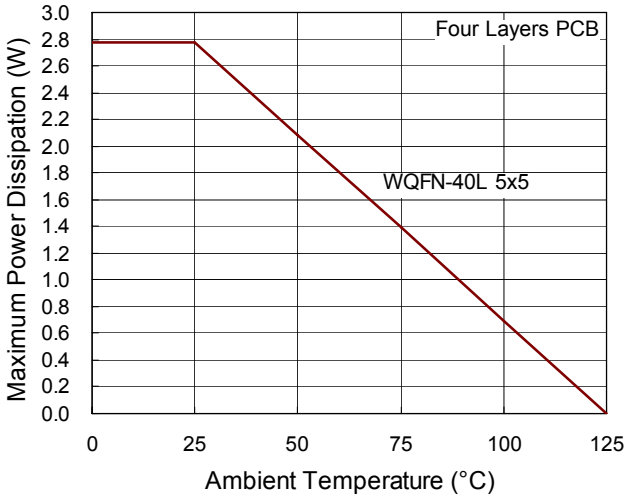


Figure 24. Derating Curves for RT9941 Packages

Layout Considerations

For the best performance of the RT9941, the following PCB Layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins.
- Keep the main power traces as possible as wide and short.
- To minimize EMI, the switching area connected to LX inductor should be smallest possible.
- Place the feedback components as close as possible to the FB pin and keep these components away from the noisy devices. Also, the feed forward capacitor C_{FF} trace is sensitive to the magnetic field that the inductor generates. Please keep the C_{FF} trace away from the inductor and use a via and run the trace between ground layers.
- Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.

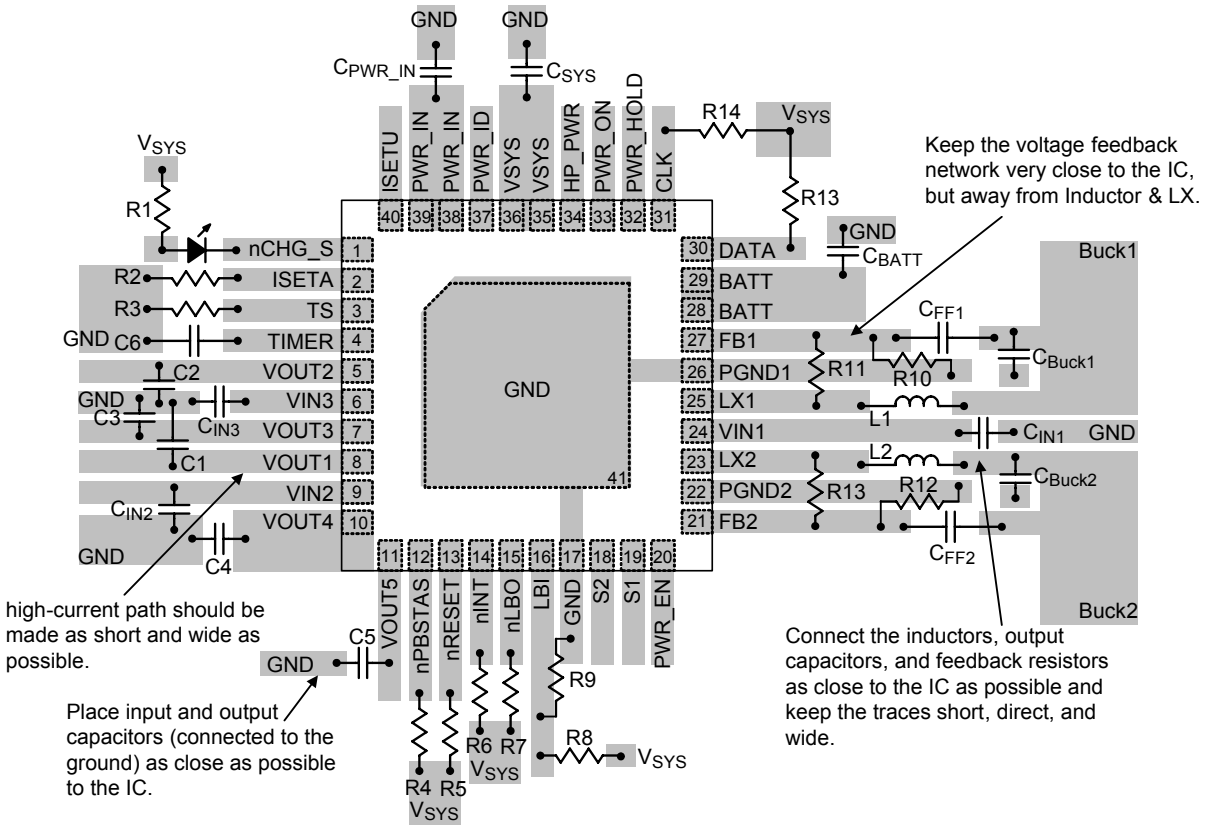
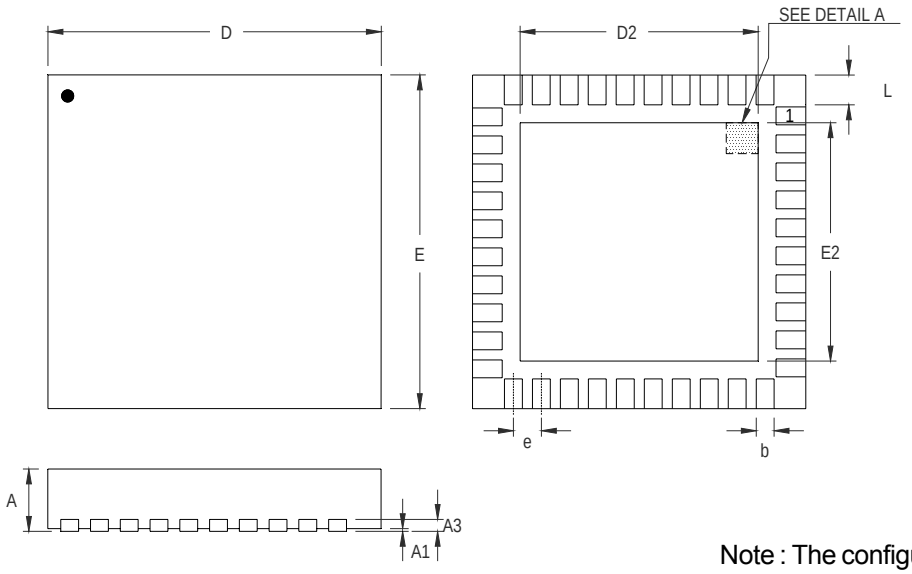
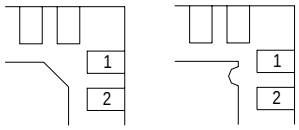


Figure 25. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

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