

# MC74LVX373

## Octal D-Type Latch with 3-State Outputs

### With 5V-Tolerant Inputs

The MC74LVX373 is an advanced high speed CMOS octal latch with 3-state outputs. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

This 8-bit D-type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

#### Features

- High Speed:  $t_{PD} = 5.8 \text{ ns}$  (Typ) at  $V_{CC} = 3.3 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4 \mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.8 \text{ V}$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant

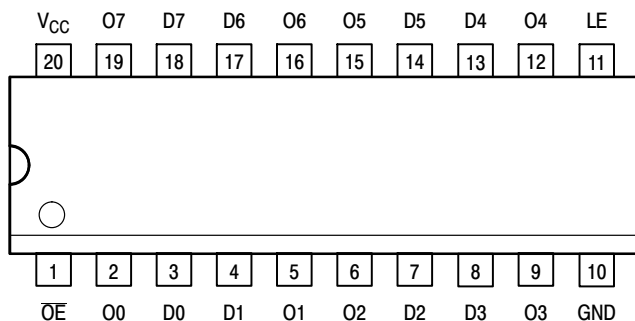


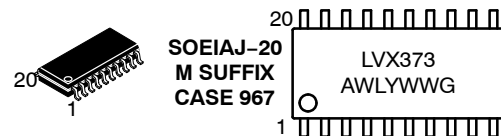
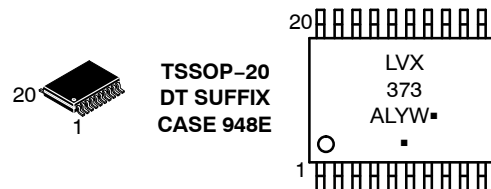
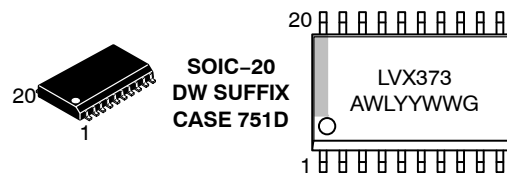
Figure 1. 20-Lead Pinout (Top View)



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#### MARKING DIAGRAMS



LVX373 = Specific Device Code  
 A = Assembly Location  
 WL, L = Wafer Lot  
 Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN NAMES

Pins	Function
OE	Output Enable Input
LE	Latch Enable Input
D0-D7	Data Inputs
O0-O7	3-State Latch Outputs

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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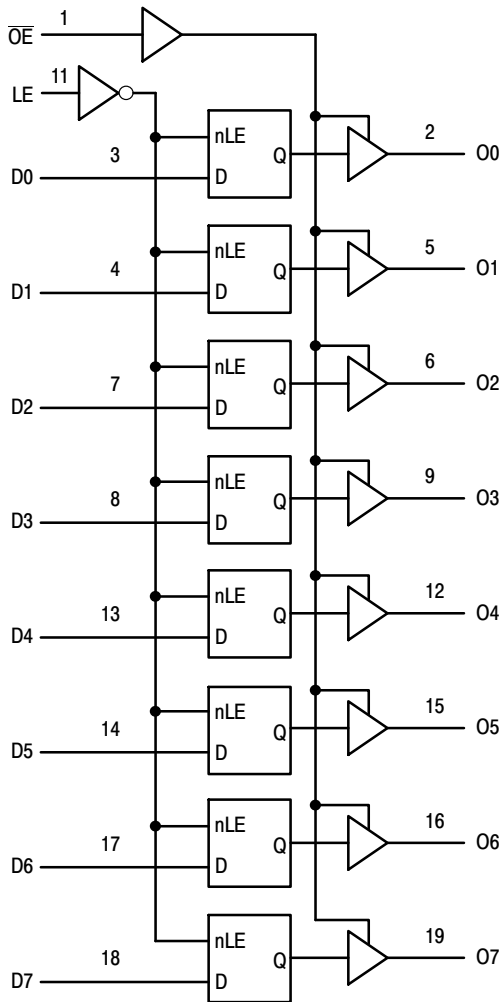


Figure 2. Logic Diagram

INPUTS			OUTPUTS	OPERATING MODE
$\overline{OE}$	LE	Dn	On	
L	H	H	H	Transparent (Latch Disabled); Read Latch
L	H	L	L	
L	L	h	H	Latched (Latch Enabled) Read Latch
L	L	l	L	
L	L	X	NC	Hold; Read Latch
H	L	X	Z	Hold; Disabled Outputs
H	H	H	Z	Transparent (Latch Disabled); Disabled Outputs
H	H	L	Z	
H	L	h	Z	Latched (Latch Enabled); Disabled Outputs
H	L	l	Z	

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition; NC = No Change, State Prior to the Latch Enable High-to-Low Transition; X = High or Low Voltage Level or Transitions are Acceptable; Z = High Impedance State; For  $I_{CC}$  Reasons DO NOT FLOAT Inputs

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
I <sub>OK</sub>	Output Diode Current	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation	180	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.0			2.0		
			3.6	2.4			2.4		
V <sub>IL</sub>	Low-Level Input Voltage		2.0			0.5		0.5	V
			3.0			0.8		0.8	
			3.6			0.8		0.8	
V <sub>OH</sub>	High-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OH</sub> = -50μA I <sub>OH</sub> = -50μA I <sub>OH</sub> = -4mA	2.0	1.9	2.0		1.9		V
			3.0	2.9	3.0		2.9		
			3.0	2.58			2.48		
V <sub>OL</sub>	Low-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OL</sub> = 50μA I <sub>OL</sub> = 50μA I <sub>OL</sub> = 4mA	2.0		0.0	0.1		0.1	V
			3.0		0.0	0.1		0.1	
			3.0			0.36		0.44	
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5V or GND	3.6			±0.1		±1.0	μA
I <sub>OZ</sub>	Maximum 3-State Leakage Current	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	3.6			±0.2 5		±2.5	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	3.6			4.0		40.0	μA

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## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay D to O	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$		7.5	14.5	1.0	17.5	ns
		$C_L = 50\text{pF}$		10.0	18.0	1.0	21.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		5.8	9.3	1.0	11.0	
		$C_L = 50\text{pF}$		8.3	12.8	1.0	14.5	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay LE to O	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$		7.7	15.0	1.0	18.5	ns
		$C_L = 50\text{pF}$		10.2	18.5	1.0	22.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		6.0	9.7	1.0	11.5	
		$C_L = 50\text{pF}$		8.5	13.2	1.0	15.0	
$t_{PZL}$ , $t_{PZH}$	Output Enable Time OE to O	$V_{CC} = 2.7\text{V}$ $R_L = 1\text{k}\Omega$		7.7	15.0	1.0	18.5	ns
		$C_L = 50\text{pF}$		10.2	18.5	1.0	22.0	
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		6.0	9.7	1.0	11.5	
		$C_L = 50\text{pF}$		8.5	13.2	1.0	15.0	
$t_{PLZ}$ , $t_{PHZ}$	Output Disable Time OE to O	$V_{CC} = 2.7\text{V}$ $R_L = 1\text{k}\Omega$		9.8	18.0	1.0	21.0	ns
		$C_L = 50\text{pF}$		8.2	12.8	1.0	14.5	
$t_{OSHL}$ , $t_{OSLH}$	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7\text{V}$ $C_L = 50\text{pF}$			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$			1.5		1.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
$C_{in}$	Input Capacitance		4	10		10	pF
$C_{out}$	Maximum Three-State Output Capacitance		6				pF
$C_{PD}$	Power Dissipation Capacitance (Note 2)		27				pF

2.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$  (per latch).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ , $C_L = 50\text{pF}$ , $V_{CC} = 3.3\text{V}$ , Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.5	0.8	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.5	-0.8	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

## TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40 \text{ to } 85^\circ\text{C}$	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	$V_{CC} = 2.7\text{V}$ $V_{CC} = 3.3 \pm 0.3\text{V}$		6.5 5.0	7.5 5.0	ns
$t_{su}$	Minimum Setup Time, D to LE	$V_{CC} = 2.7\text{V}$ $V_{CC} = 3.3 \pm 0.3\text{V}$		6.0 4.0	6.0 4.0	ns
$t_h$	Minimum Hold Time, D to LE	$V_{CC} = 2.7\text{V}$ $V_{CC} = 3.3 \pm 0.3\text{V}$		1.0 1.0	1.0 1.0	ns

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## ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX373DWR2G	SOIC-20 (Pb-Free)	1000 Tape & Reel
MC74LVX373DTR2G	TSSOP-20*	2500 Tape & Reel
MC74LVX373MG	SOEIAJ-20 (Pb-Free)	50 Units / Rail
MC74LVX373MELG	SOEIAJ-20 (Pb-Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

## SWITCHING WAVEFORMS

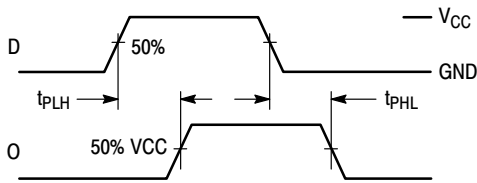


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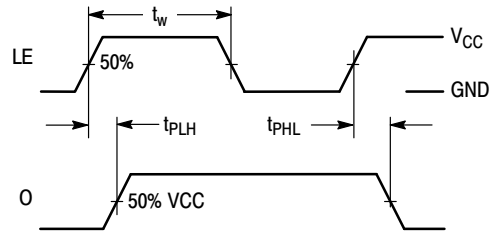


Figure 4.

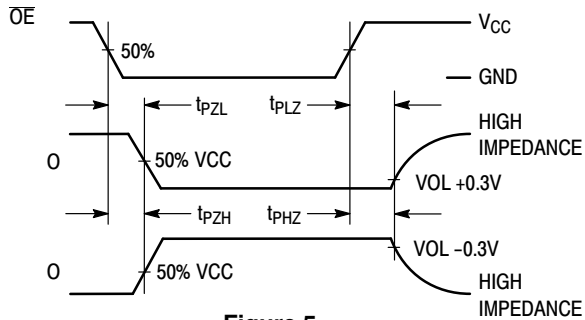


Figure 5.

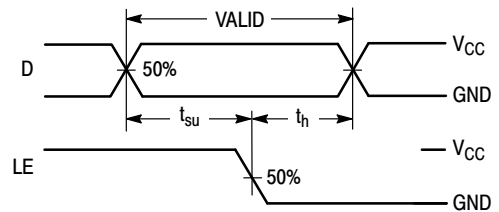
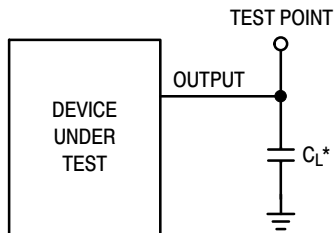


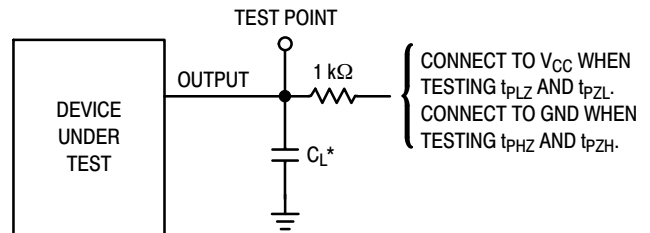
Figure 6.

## TEST CIRCUITS



\*Includes all probe and jig capacitance

Figure 7. Propagation Delay Test Circuit



\*Includes all probe and jig capacitance

Figure 8. Three-State Test Circuit

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## PACKAGE DIMENSIONS

SOIC-20  
CASE 751D-05  
ISSUE G

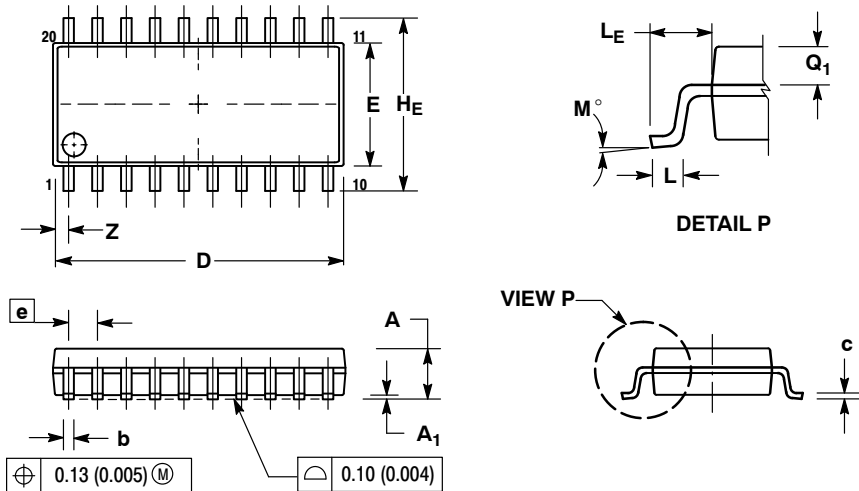


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

SOEIAJ-20  
CASE 967-01  
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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## PACKAGE DIMENSIONS

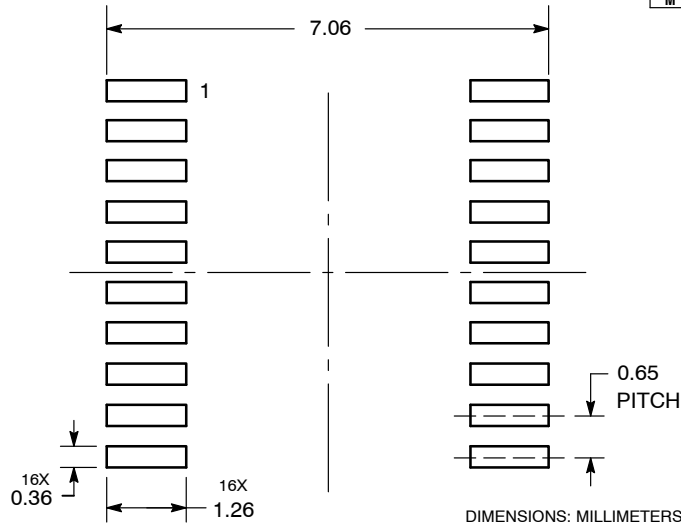
TSSOP-20  
CASE 948E-02  
ISSUE C



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



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