Freescale Semiconductor
Advance Information

MPC853TEC
Rev. 1, 12/2004

MPC853T Hardware Specification

This hardware specification contains detailed information on the power considerations, DC/AC electrical characteristics, and AC timing specifications of the MPC853T. The MPC853T contains a PowerPC™ processor core.

This hardware specification describes pertinent electrical and physical characteristics of the MPC853T. For the functional characteristics of the processor, refer to the *MPC866 PowerQUICC™ Family User's Manual* (MPC866UM).

Contents

1 Overview

The MPC853T PowerQUICC™ is a 0.18-micron derivative of the MPC860 PowerQUICC family. It can operate at up to 100 MHz on the MPC8xx core with a 66-MHz external bus. The MPC853T has a 1.8-V core and 3.3-V I/O operation with 5-V TTL compatibility. The MPC853T integrated communications controller is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in Ethernet control applications, including CPE equipment, Ethernet routers and hubs, VoIP clients, and Wi-Fi access points.

The MPC853T is a PowerPC architecture-based derivative of Freescale's MPC860 quad integrated communications controller (PowerQUICC). The CPU on the MPC853T has a MPC8xx core, a 32-bit microprocessor that implements the PowerPC architecture

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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and incorporates memory management units (MMUs), instruction and data caches. The MPC853T is a subset of this family of devices and is the main focus of this document.

2 Features

The MPC853T is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM). The MPC853T block diagram is shown in Figure 1.

The following list summarizes the key MPC853T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - The 50-/66-MHz core frequencies support both the 1:1 and 2:1 modes.
  - The 80-/100-MHz core frequencies support 2:1 mode only.
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch and without conditional execution.
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - Instruction cache is two-way, set-associative with 128 sets
    - Data cache is two-way, set-associative with 128 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry translation look-aside buffer (TLB), fully associative instruction, and data TLBs
  - MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank.
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- Fast Ethernet Controller (FEC)

- General-purpose timers
  - Two 16-bit timers or one 32-bit timer
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Clock synthesizer
  - Decrementer and time base
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - Seven port pins with interrupt capability
  - Eighteen internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - Eight serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- Two baud-rate generators
  - Independent (can be connected to any SCC3/4 or SMC1)
  - Allow changes during operation
  - Autobaud support option
- Two SCCs (serial communication controllers)
  - Ethernet/IEEE 802.3 optional on SCC3 & SCC4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Universal asynchronous receiver transmitter (UART)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- SMC (serial management channels)
  - UART

- SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- The MPC853T has a time-slot assigner (TSA) that supports one TDM bus (TDMb)
  - Allows SCCs and SMC to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - Can be internally connected to three serial channels (two SCCs and one SMC)
- PCMCIA interface
  - Master (socket) interface, release 2.1 compliant
  - Supports one independent PCMCIA socket, 8 memory or I/O windows
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- Normal high and normal low power modes to conserve power
- 1.8-V core and 3.3-V I/O operation with 5-V TTL compatibility. Refer to Table 5 for a listing of the 5-V tolerant pins.

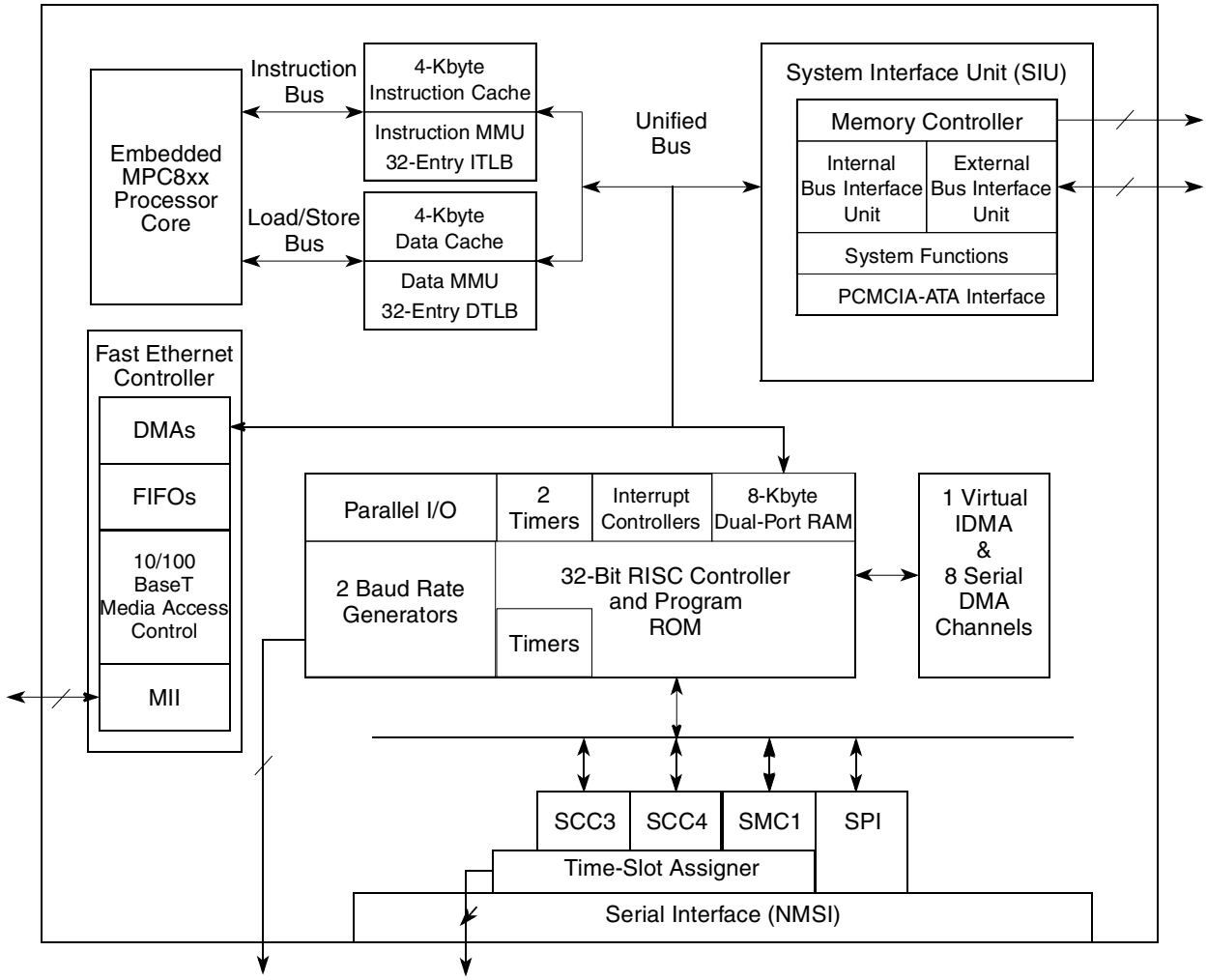


Figure 1. MPC853T Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC853T. Table 1 provides the maximum ratings and the operating temperatures.

Table 1. Maximum Tolerated Ratings

Rating	Symbol	Value	Unit
Supply voltage [1]	V_{DDL} (core voltage)	–0.3 to 3.4	V
	V_{DDH} (I/O voltage)	–0.3 to 4	V
	V_{DDSYN}	–0.3 to 3.4	V
	Difference between V_{DDL} and V_{DDSYN}	100	mV
Input voltage [2]	V_{in}	GND–0.3 to V_{DDH}	V
Storage temperature range	T_{stg}	–55 to +150	°C

[1] The power supply of the device must start its ramp from 0.0 V.

[2] Functional operating conditions are provided with the DC electrical specifications in Table 5. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH}. This restriction applies to power up and normal operation (that is, if the MPC853T is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Table 2. Operating Temperatures

Rating	Symbol	Value	Unit
Temperature [1] (standard)	$T_{A(min)}$	0	°C
	$T_{j(max)}$	95	°C
Temperature (extended)	$T_{A(min)}$	–40	°C
	$T_{j(max)}$	100	°C

[1] Minimum temperatures are guaranteed as ambient temperature, T_A. Maximum temperatures are guaranteed as junction temperature, T_j.

This device contains circuitry protecting against damage caused by high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND, V_{DDL}, or V_{DDH}).

4 Thermal Characteristics

Table 3 shows the thermal characteristics for the MPC853T.

Table 3. MPC853T Thermal Resistance Data

Rating	Environment		Symbol	Value	Unit
Junction-to-ambient [1]	Natural convection	Single-layer board (1s)	$R_{\theta JA}$ [2]	49	°C/W
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	32	
	Airflow (200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$ [3]	41	
		Four-layer board (2s2p)	$R_{\theta JMA}$ [3]	29	
Junction-to-board [4]			$R_{\theta JB}$	24	
Junction-to-case [5]			$R_{\theta JC}$	13	
Junction-to-package top [6]	Natural convection		Ψ_{JT}	3	
	Airflow (200 ft/min)		Ψ_{JT}	2	

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5 Power Dissipation

Table 4 provides power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice bus speed.

Table 4. Power Dissipation (P_D)

Die Revision	Bus Mode	Frequency (MHz)	Typical [1]	Maximum [2]	Unit
0	1:1	50	110	140	mW
		66	150	180	mW
	2:1	66	140	160	mW
		80	170	200	mW
		100	210	250	mW

1 Typical power dissipation is measured at 1.9 V.

2 Maximum power dissipation at V_{DDL} and V_{DDSYN} is at 1.9 V, and V_{DDH} is at 3.465 V.

NOTE

Values in Table 4 represent V_{DDL}-based power dissipation and do not include I/O power dissipation over V_{DDH}. I/O power dissipation varies widely by application due to buffer current, which depends on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 5 provides the DC electrical characteristics for the MPC853T.

Table 5. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Operating voltage	V_{DDH}	3.135	3.465	V
	V_{DDL}	1.7	1.9	V
	V_{DDSYN}	1.7	1.9	V
	Difference between V_{DDL} and V_{DDSYN}	—	100	mV
Input high voltage (all inputs except PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{\text{TRST}}$, TMS, MII_TXEN, MII_MDIO) [1]	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
EXTAL, EXTCLK input high voltage	V_{IHC}	$0.7 \times V_{DDH}$	V_{DDH}	V
Input leakage current, Vin = 5.5 V (except the TMS, $\overline{\text{TRST}}$, DSCK, and DSDI pins) for 5-V tolerant pins [1]	I_{in}	—	100	µA
Input leakage current, Vin = V_{DDH} (except TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input leakage current, Vin = 0 V (except the TMS, $\overline{\text{TRST}}$, DSCK, and DSDI)	I_{In}	—	10	µA
Input capacitance [2]	C_{in}	—	20	pF

Table 5. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Output high voltage, IOH = –2.0 mA, V_{DDH} = 3.0 V (except XTAL and open-drain pins)	V_{OH}	2.4	—	V
Output low voltage IOL = 2.0 mA (CLKOUT) IOL = 3.2 mA [3] IOL = 5.3 mA [4] IOL = 7.0 mA (Txd1/pa14, txd2/pa12) IOL = 8.9 mA ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{HRESET}$, $\overline{SRESET}$)	V_{OL}	—	0.5	V

1 The PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15, PD[3:15], TDI, TDO, TCK, $\overline{TRST}$, TMS, MII_TXEN, and MII_MDIO are 5-V tolerant pins.

2 Input capacitance is periodically sampled.

3 A(0:31), TSIZ0/$\overline{REG}$, TSIZ1, D(0:31), DP(0:3)/$\overline{IRQ}$(3:6), RD/$\overline{WR}$, $\overline{BURST}$, $\overline{RSV}$/$\overline{IRQ2}$, IWP(0:1)/VFLS(0:1), RXD3/PA11, TXD3/PA10, RXD4/PA9, TXD4/PA8, TIN3/BRGO3/CLK5/PA3, BRGCLK2/$\overline{TOUT3}$/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, $\overline{TOUT4}$/CLK8/PA0, $\overline{SPISEL}$/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, SMTXD1/PB25, SMRXD1/PB24, BRGO3/PB15, $\overline{RTS1}$/$\overline{DREQ0}$/PC15, $\overline{RTS3}$/PC13, $\overline{RTS4}$/PC12, $\overline{CTS3}$/PC7, $\overline{CD3}$/PC6, $\overline{CTS4}$/$\overline{SDACK1}$/PC5, $\overline{CD4}$/PC4, MII-RXD3/PD15, MII-RXD2/PD14, MII-RXD1/PD13, MII-MDC/PD12, MII-TXERR/RXD3/PD11, MII-RX0/TXD3/PD10, MII-TXD0/RXD4/PD9, MII-RXCLK/TXD4/PD8, MII-TXD3/PD5, MII-RXDV/$\overline{RTS4}$/PD6, MII-RXERR/$\overline{RTS3}$/PD7, MII-TXD2/REJECT3/PD4, MII-TXD1/REJECT4/PD3, MII_CRS, MII_MDIO, MII_TXEN, MII_COL

4 $\overline{BDIP}$/$\overline{GPL\_B}$(5), $\overline{BR}$, $\overline{BG}$, FRZ/$\overline{IRQ6}$, $\overline{CS}$(0:5), $\overline{CS}$(6), $\overline{CS}$(7), $\overline{WE0}$/BS_B0/$\overline{IORD}$, $\overline{WE1}$/BS_B1/$\overline{IOWR}$, $\overline{WE2}$/BS_B2/$\overline{PCOE}$, $\overline{WE3}$/ BS_B3/$\overline{PCWE}$, $\overline{BS}$_A(0:3), $\overline{GPL\_A0}$/$\overline{GPL\_B0}$, $\overline{OE}$/$\overline{GPL\_A1}$/$\overline{GPL\_B1}$, $\overline{GPL\_A}$(2:3)/$\overline{GPL\_B}$(2:3)/$\overline{CS}$(2:3), UPWAITA/$\overline{GPL\_A4}$, $\overline{GPL\_A5}$, ALE_A, $\overline{CE}$1_A, $\overline{CE}$2_A, DSCK, OP(0:1), OP2/MODCK1/$\overline{STS}$, OP3/MODCK2/DSDO, BADDR(28:30)

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature ºC

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, and especially PBGA packages, is strongly dependent on the board temperature. If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

T_B = board temperature ºC

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used. It determines the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per the JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC853T power supply. The MPC853T has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at lower voltages than the I/O voltage V_{DDH}. The I/O section of the MPC853T is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:3], PA[8:11], PB15, PB[24:25]; PB[28:31], PC[4:7], PC[12:13], PC15] PD[3:15], TDI, TDO, TCK, TRST, TMS, MII_TXEN, and MII_MDIO are 5-V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH}. In addition, 5-V tolerant pins can not exceed 5.5 V, and remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 2 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up and the 1N5820 diodes regulate the maximum potential difference on power down.

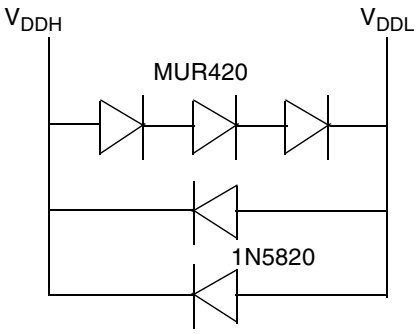


Figure 2. Example Voltage Sequencing Circuit

9 Mandatory Reset Configurations

The MPC853T requires a mandatory configuration during reset.

If hardware reset configuration word (HRCW) is enabled, the HRCW[DBGC] value needs to be set to binary X1 in HRCW, and the SIUMCR[DBGC] should be programmed with the same value in the boot code after reset. This can be done by asserting the $\overline{\text{RSTCONF}}$ during $\overline{\text{HRESET}}$ assertion.

If HRCW is disabled, the SIUMCR[DBGC] should be programmed with binary X1 in the boot code after reset by negating the $\overline{\text{RSTCONF}}$ during the $\overline{\text{HRESET}}$ assertion.

The MBMR[GPLB4DIS], PAPAR, PADIR, PBPAR, PBDIR, PCPAR, and PCDIR registers need to be configured with the mandatory value in Table 6 in the boot code after the reset is negated.

Table 6. Mandatory Reset Configuration of MPC853T

Register/Configuration	Field	Value (binary)
HRCW (Hardware reset configuration word)	HRCW[DBGC]	0bx1
SIUMCR (SIU module configuration register)	SIUMCR[DBGC]	0bx1
MBMR (Machine B mode register)	MBMR[GPLB4DIS}	0
PAPAR (Port A pin assignment register)	PAPAR[4:7] PAPAR[12:15]	0
PADIR (Port A data direction register)	PADIR[4:7] PADIR[12:15]	1
PBPAR (Port B pin assignment register)	PBPAR[14] PBPAR[16:23] PBPAR[26:27]	0
PBDIR (Port B Data direction register)	PBDIR[14] PBDIR[16:23] PBDIR[26:27]	1

Table 6. Mandatory Reset Configuration of MPC853T (continued)

Register/Configuration	Field	Value (binary)
PCPAR (Port C pin assignment register)	PCPAR[8:11] PCDIR[14]	0
PCDIR (Port C data direction register)	PCDIR[8:11] PCDIR[14]	1

10 Layout Practices

Each V_{DD} pin on the MPC853T should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1-µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized, and additional appropriate decoupling capacitors should be used if required. Capacitor leads and associated printed circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC853T have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads, as well as parasitic capacitances caused by the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN}, V_{SSSYN}, V_{SSSYN1})" in the *MPC866 PowerQUICC Family User's Manual*.

11 Bus Signal Timing

The maximum bus speed supported by the MPC853T is 66 MHz. Table 7 shows the frequency ranges for standard part frequencies in 1:1 bus mode.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

Part Frequency	50 MHz		66 MHz	
	Min	Max	Min	Max
Core Frequency	40	50	40	66.67
Bus Frequency	40	50	40	66.67

Table 8 shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

Part Frequency	50 MHz		66 MHz		80 MHz		100 MHz	
	Min	Max	Min	Max	Min	Max	Min	Max
Core Frequency	40	50	40	66.67	40	80	40	100
Bus Frequency 2:1	20	25	20	33.33	20	40	20	50

Table 9 provides the bus operation timing for the MPC853T at 33, 40, 50, and 66 MHz.

The timing for the MPC853T bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay.

Table 9. Bus Operation Timings

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B1	Bus period (CLKOUT), see Table 7	—	—	—	—	—	—	—	—	ns
B1a	EXTCLK to CLKOUT phase skew - If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.	–2	+2	–2	+2	–2	+2	–2	+2	ns
B1b	CLKOUT frequency jitter peak-to-peak	—	1	—	1	—	1	—	1	ns
B1c	Frequency jitter on EXTCLK [1]	—	0.50	—	0.50	—	0.50	—	0.50	%
B1d	CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz	—	4	—	4	—	4	—	4	ns
	CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz	—	5	—	5	—	5	—	5	ns
B2	CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B3	CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1)	12.1	18.2	10.0	15.0	8.0	12.0	6.1	9.1	ns
B4	CLKOUT rise time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B5	CLKOUT fall time	—	4.00	—	4.00	—	4.00	—	4.00	ns
B7	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B7a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B7b	CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 × B1)	7.60	—	6.30	—	5.00	—	3.80	—	ns
B8	CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8a	CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, $\overline{BDIP}$, PTR valid (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B8b	CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [3] (MAX = 0.25 × B1 + 6.3)	—	13.80	—	12.50	—	11.30	—	10.00	ns
B9	CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, PTR High-Z (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B11	CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 × B1 + 6.0)	7.60	13.60	6.30	12.30	5.00	11.00	3.80	9.80	ns
B11a	CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30 [2])	2.50	9.30	2.50	9.30	2.50	9.30	2.50	9.80	ns
B12	CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 × B1 + 4.8)	7.60	12.30	6.30	11.00	5.00	9.80	3.80	8.50	ns
B12a	CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B13	CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 × B1)	7.60	21.60	6.30	20.30	5.00	19.00	3.80	14.00	ns
B13a	CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B14	CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 × B1 + 9.00)	2.50	9.00	2.50	9.00	2.50	9.00	2.50	9.00	ns
B15	CLKOUT to $\overline{TEA}$ High-Z (MIN = 0.00 × B1 + 2.50)	2.50	15.00	2.50	15.00	2.50	15.00	2.50	15.00	ns
B16	$\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B16a	$\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5)	4.50	—	4.50	—	4.50	—	4.50	—	ns
B16b	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time) [3] (4MIN = 0.00 × B1 + 0.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B17	CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time) (MIN = 0.00 × B1 + 1.00 [4])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B17a	CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B18	D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) [5] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B19	CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) [5] (MIN = 0.00 × B1 + 1.00 [6])	1.00	—	1.00	—	1.00	—	2.00	—	ns
B20	D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) [7](MIN = 0.00 × B1 + 4.00)	4.00	—	4.00	—	4.00	—	4.00	—	ns
B21	CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) [7] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B22	CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22a	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 × B1 + 8.00)	—	8.00	—	8.00	—	8.00	—	8.00	ns
B22b	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 × B1 + 6.3)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B22c	CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	16.00	7.00	14.10	5.20	12.30	ns
B23	CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 × B1 + 8.00)	2.00	8.00	2.00	8.00	2.00	8.00	2.00	8.00	ns
B24	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B24a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B25	CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3)/BS_B[0:3] asserted (MAX = 0.00 × B1 + 9.00)	—	9.00		9.00		9.00		9.00	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B26	CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 × B1 + 9.00)	2.00	9.00	2.00	9.00	2.00	9.00	2.00	9.00	ns
B27	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00)	35.90	—	29.30	—	23.00	—	16.90	—	ns
B27a	A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B28	CLKOUT rising edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access CSNT = 0 (MAX = 0.00 × B1 + 9.00)	—	9.00	—	9.00	—	9.00	—	9.00	ns
B28a	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B28b	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	—	14.30	—	13.00	—	11.80	—	10.50	ns
B28c	CLKOUT falling edge to $\overline{WE}$(0:3)/BS_B[0:3] negated GPCM write access TRLX = 0,1 CSNT = 1 write access TRLX = 0,1 CSNT = 1, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	10.90	18.00	10.90	18.00	7.00	14.30	5.20	12.30	ns
B28d	CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1 CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 × B1 + 6.6)	—	18.00	—	18.00	—	14.30	—	12.30	ns
B29	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B29a	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29b	$\overline{CS}$ negated to D(0:31), DP(0:3), High-Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B29c	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B29d	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29e	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns
B29f	$\overline{WE}$(0:3/BS_B[0:3]) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29g	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 6.30)	5.00	—	3.00	—	1.10	—	0.00	—	ns
B29h	$\overline{WE}$(0:3)/BS_B[0:3] negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B29i	$\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 × B1 – 3.30)	38.40	—	31.10	—	24.20	—	17.50	—	ns
B30	$\overline{CS}$, $\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access [8] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B30a	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B30b	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31) Invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 × B1 – 2.00)	43.50	—	35.50	—	28.00	—	20.70	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B30c	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 × B1 – 3.00)	8.40	—	6.40	—	4.50	—	2.70	—	ns
B30d	$\overline{WE}$(0:3)/BS_B[0:3] negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1	38.67	—	31.38	—	24.50	—	17.83	—	ns
B31	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B31a	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B31b	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns
B31c	CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
B31d	CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 × B1 + 6.6)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B32	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B32a	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32b	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 × B1 + 8.00)	1.50	8.00	1.50	8.00	1.50	8.00	1.50	8.00	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B32c	CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B32d	CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 × B1 + 6.60)	13.30	18.00	11.30	16.00	9.40	14.10	7.60	12.30	ns
B33	CLKOUT falling edge to $\overline{GPL}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 × B1 + 6.00)	1.50	6.00	1.50	6.00	1.50	6.00	1.50	6.00	ns
B33a	CLKOUT rising edge to $\overline{GPL}$ valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 × B1 + 6.80)	7.60	14.30	6.30	13.00	5.00	11.80	3.80	10.50	ns
B34	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B34a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B34b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B35	A(0:31), BADDR(28:30) to $\overline{CS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
B35a	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by BST1 in the corresponding word in the UPM (MIN = 0.50 × B1 – 2.00)	13.20	—	10.50	—	8.00	—	5.60	—	ns
B35b	A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
B36	A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns

Table 9. Bus Operation Timings (continued)

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
B37	UPWAIT valid to CLKOUT falling edge [9] (MIN = 0.00 × B1 + 6.00)	6.00	—	6.00	—	6.00	—	6.00	—	ns
B38	CLKOUT falling edge to UPWAIT valid [9] (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns
B39	$\overline{AS}$ valid to CLKOUT rising edge [10] (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B40	A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B41	$\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 × B1 + 7.00)	7.00	—	7.00	—	7.00	—	7.00	—	ns
B42	CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns
B43	$\overline{AS}$ negation to memory controller signals negation (MAX = TBD)	—	TBD	—	TBD	—	TBD	—	TBD	ns

1 If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time) the maximum allowed jitter on EXTAL can be up to 2%.

2 For part speeds above 50 MHz, use 9.80 ns for B11a.

3 The timing required for $\overline{BR}$ input is relevant when the MPC853T is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC853T is selected to work with the external bus arbiter.

4 For part speeds above 50 MHz, use 2 ns for B17.

5 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the $\overline{TA}$ input signal is asserted.

6 For part speeds above 50 MHz, use 2 ns for B19.

7 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.

8 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

9 The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 18.

10 The $\overline{AS}$ signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 21.

Figure 3 provides the control timing diagram.

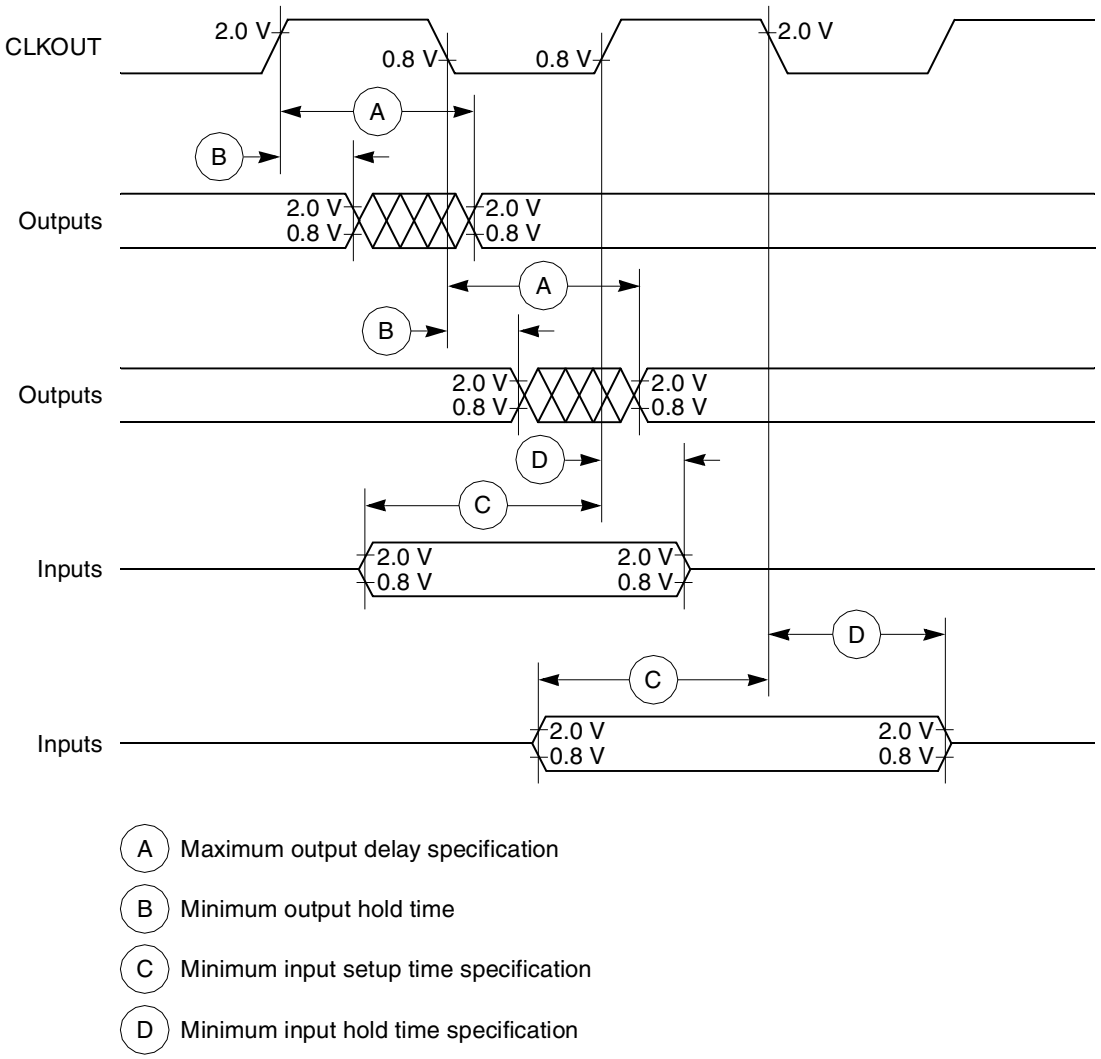


Figure 3. Control Timing

Figure 4 provides the timing for the external clock.

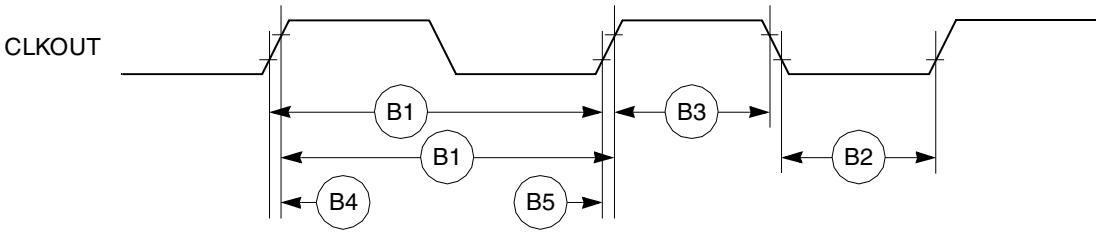


Figure 4. External Clock Timing

Figure 5 provides the timing for the synchronous output signals.

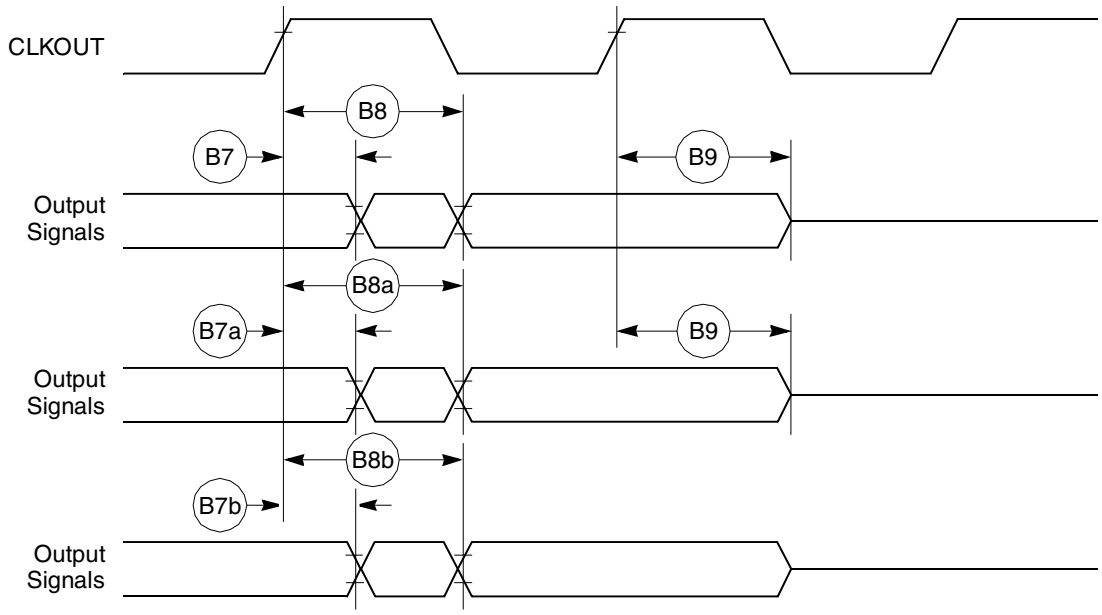


Figure 5. Synchronous Output Signals Timing

Figure 6 provides the timing for the synchronous active pull-up and open-drain output signals.

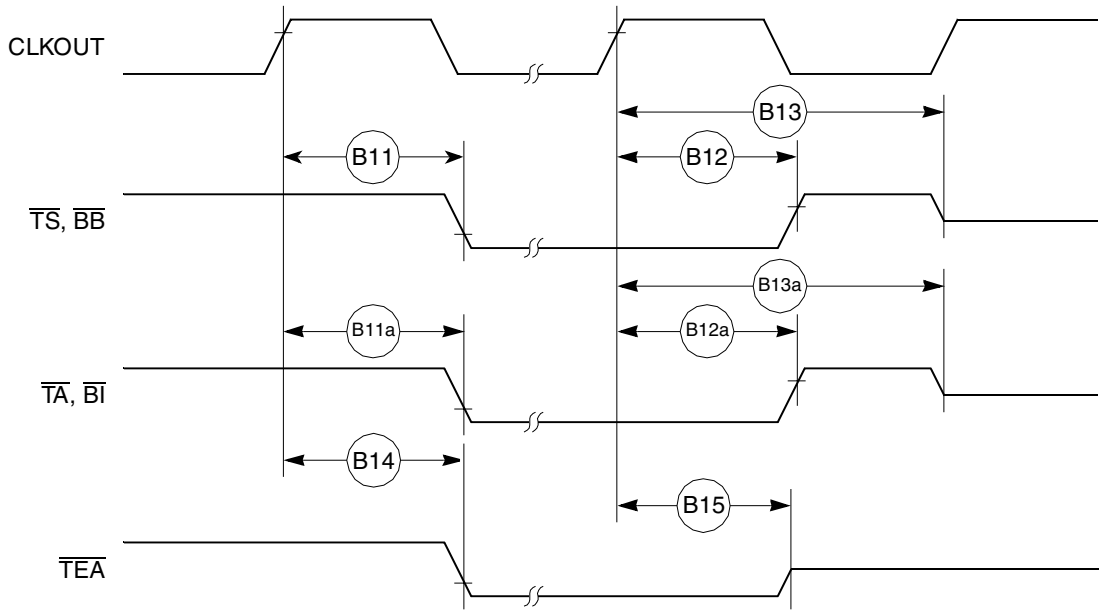


Figure 6. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 7 provides the timing for the synchronous input signals.

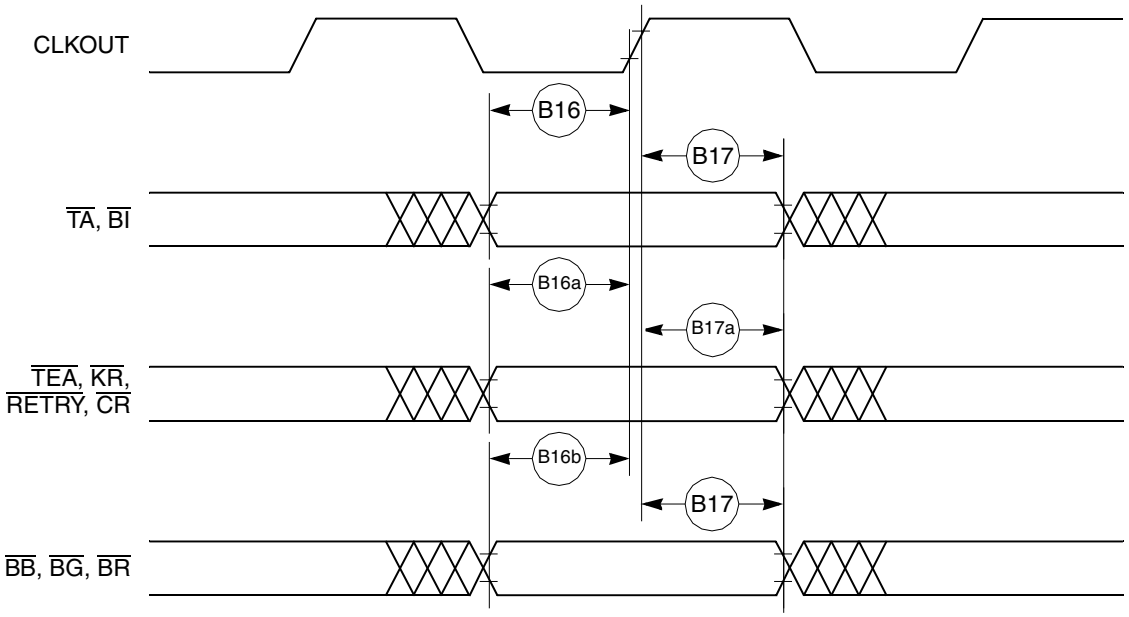


Figure 7. Synchronous Input Signals Timing

Figure 8 provides normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

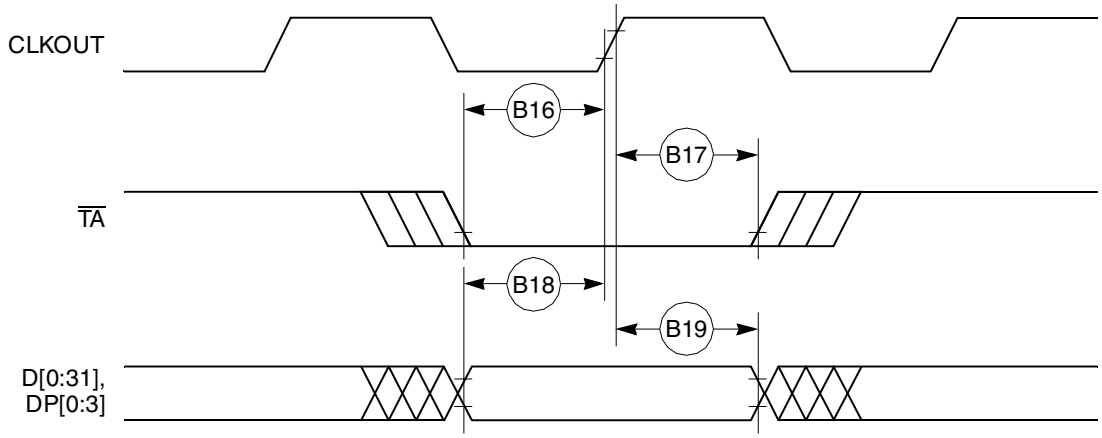


Figure 8. Input Data Timing in Normal Case

Figure 9 provides the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

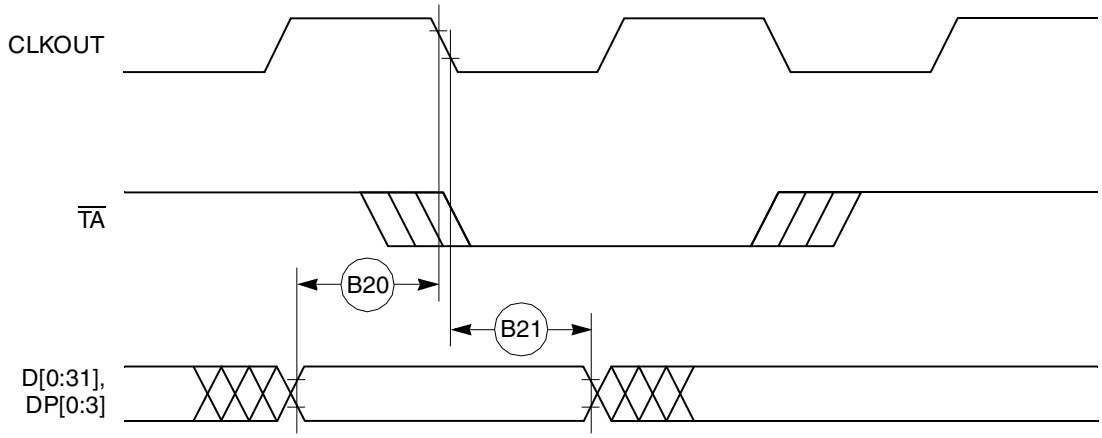


Figure 9. Input Data Timing When Controlled by the UPM in the Memory Controller and DLT3 = 1

Figure 10 through Figure 13 provide the timing for the external bus read controlled by various GPCM factors.

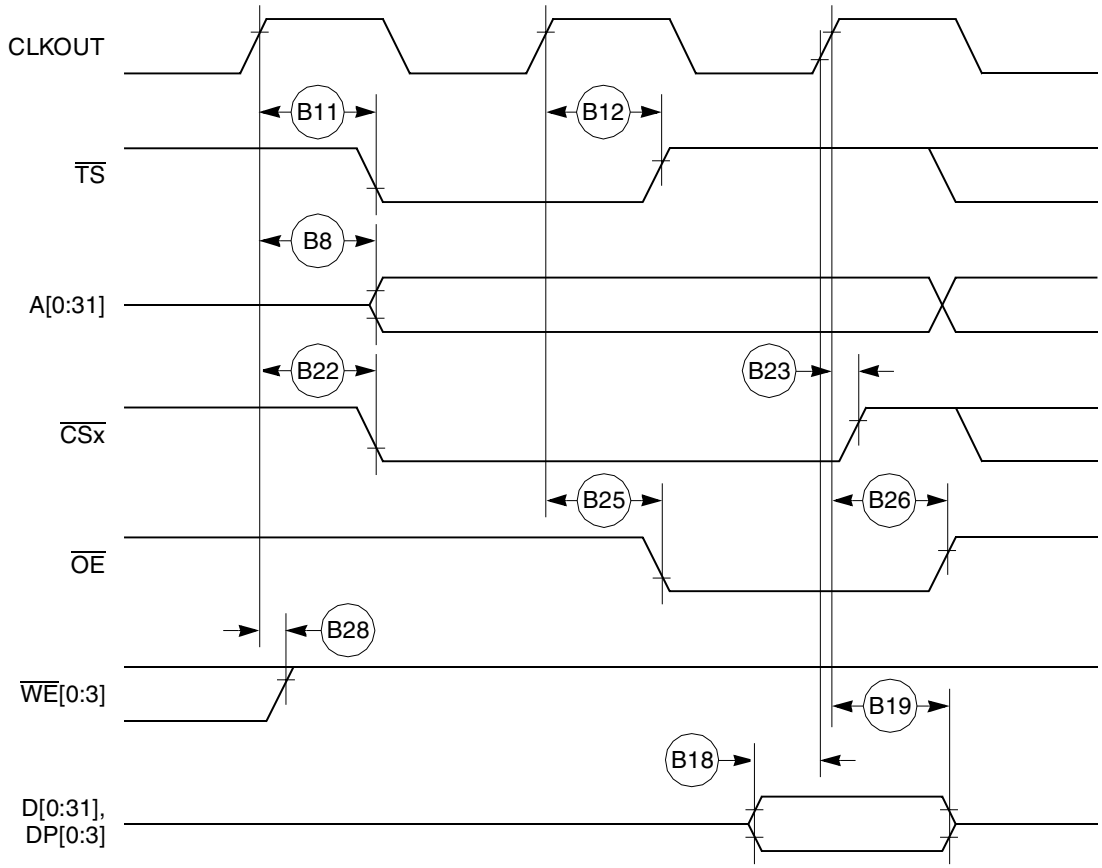


Figure 10. External Bus Read Timing (GPCM Controlled—ACS = 00)

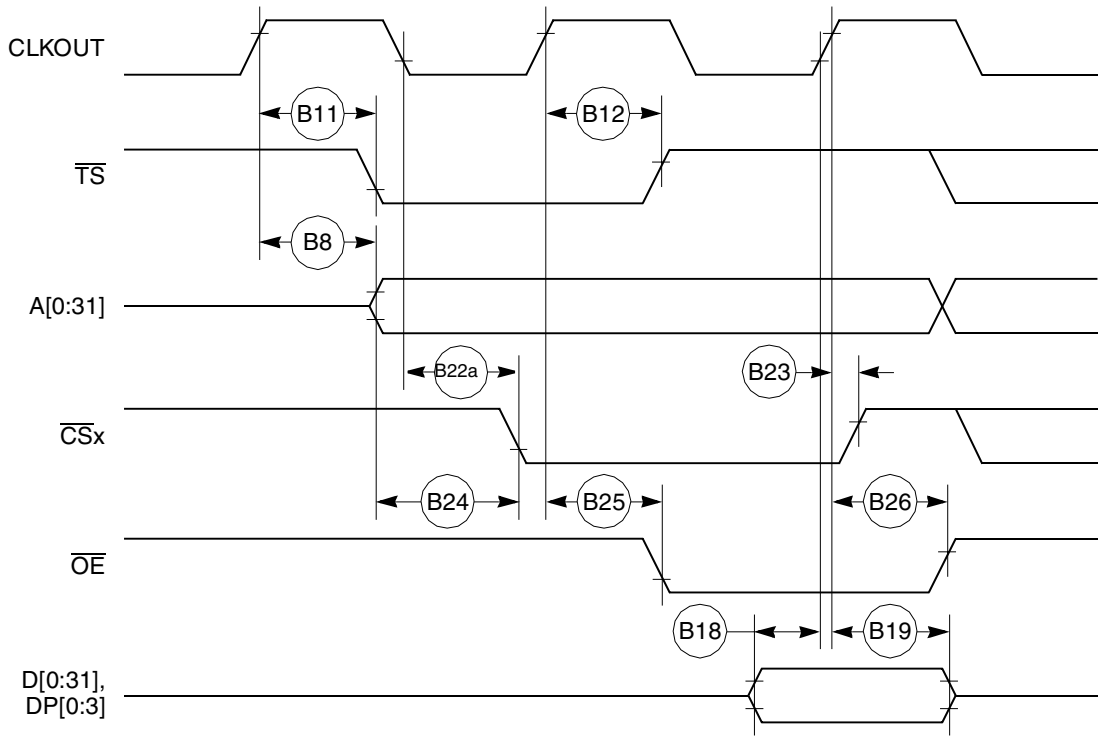


Figure 11. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

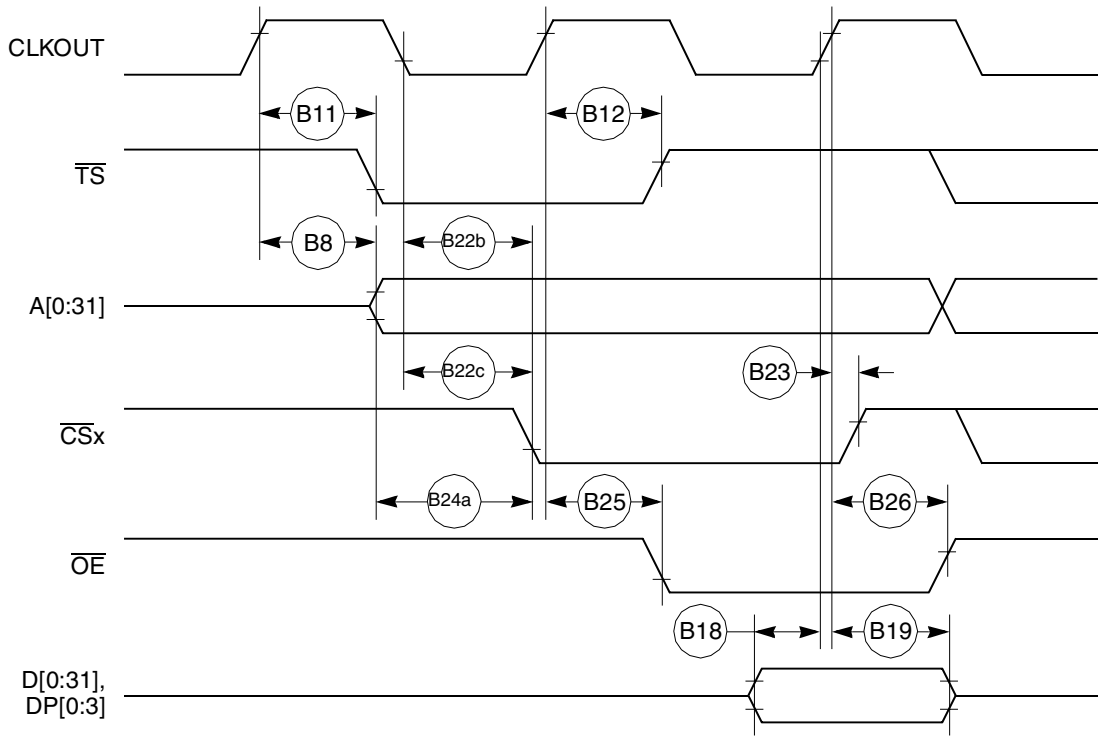


Figure 12. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

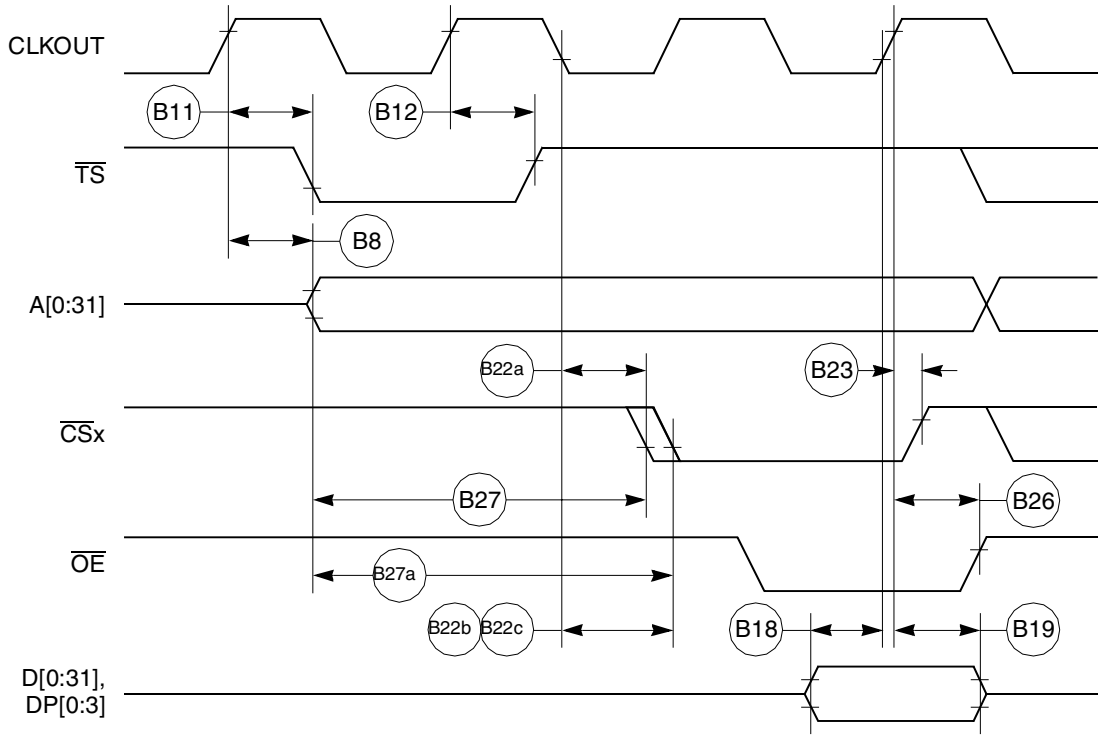


Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)

Figure 14 through Figure 16 provide the timing for the external bus write controlled by various GPCM factors.

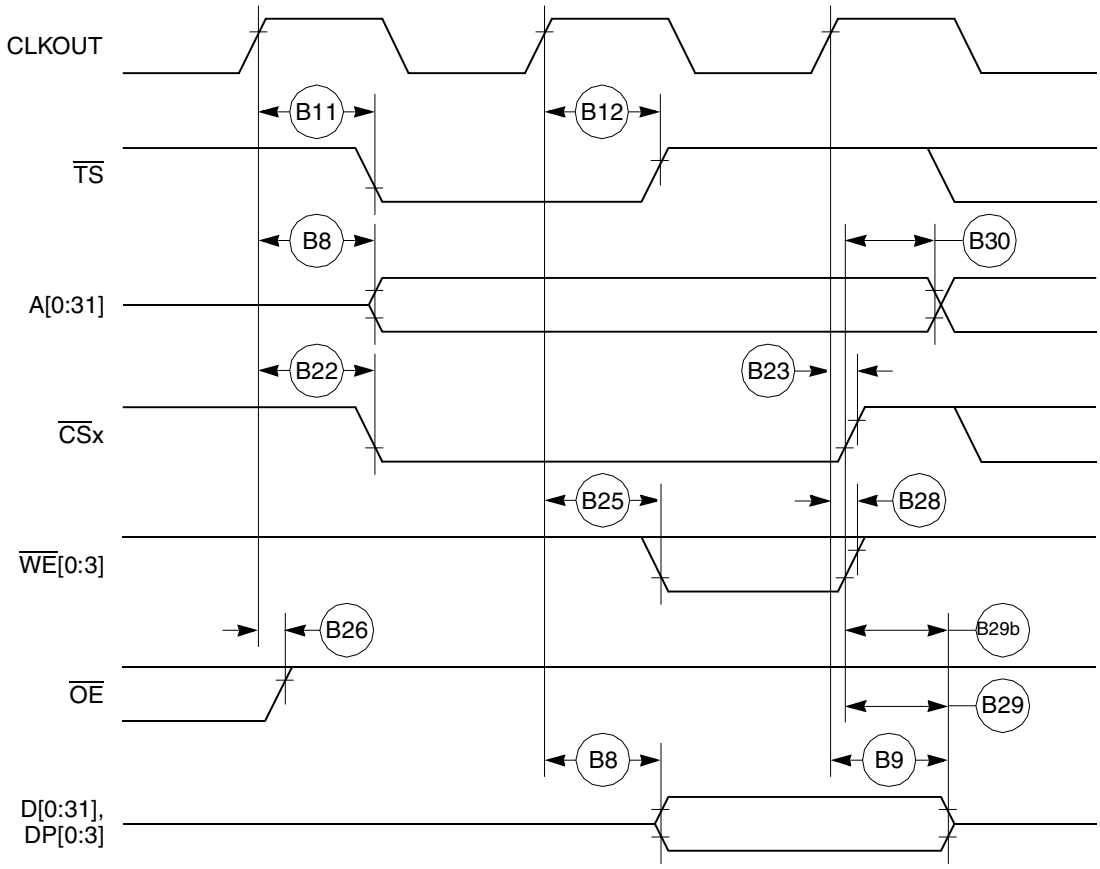


Figure 14. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)

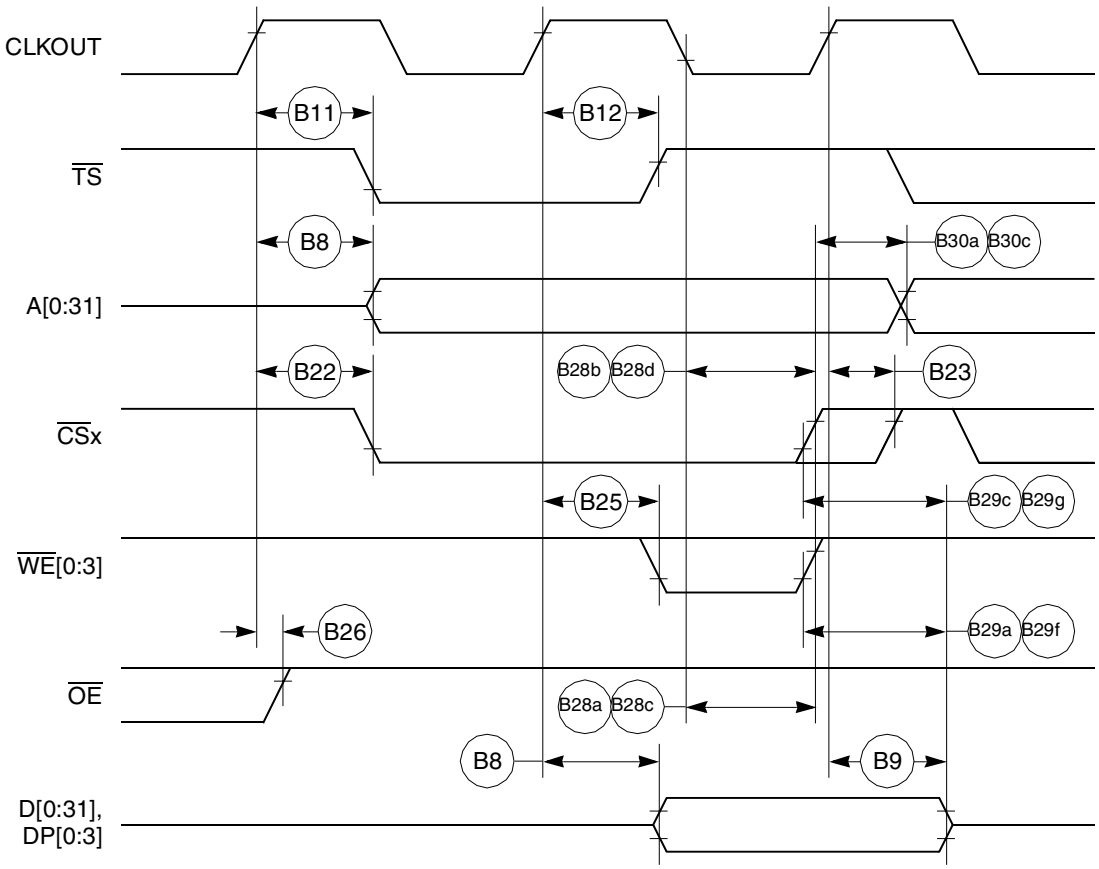


Figure 15. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

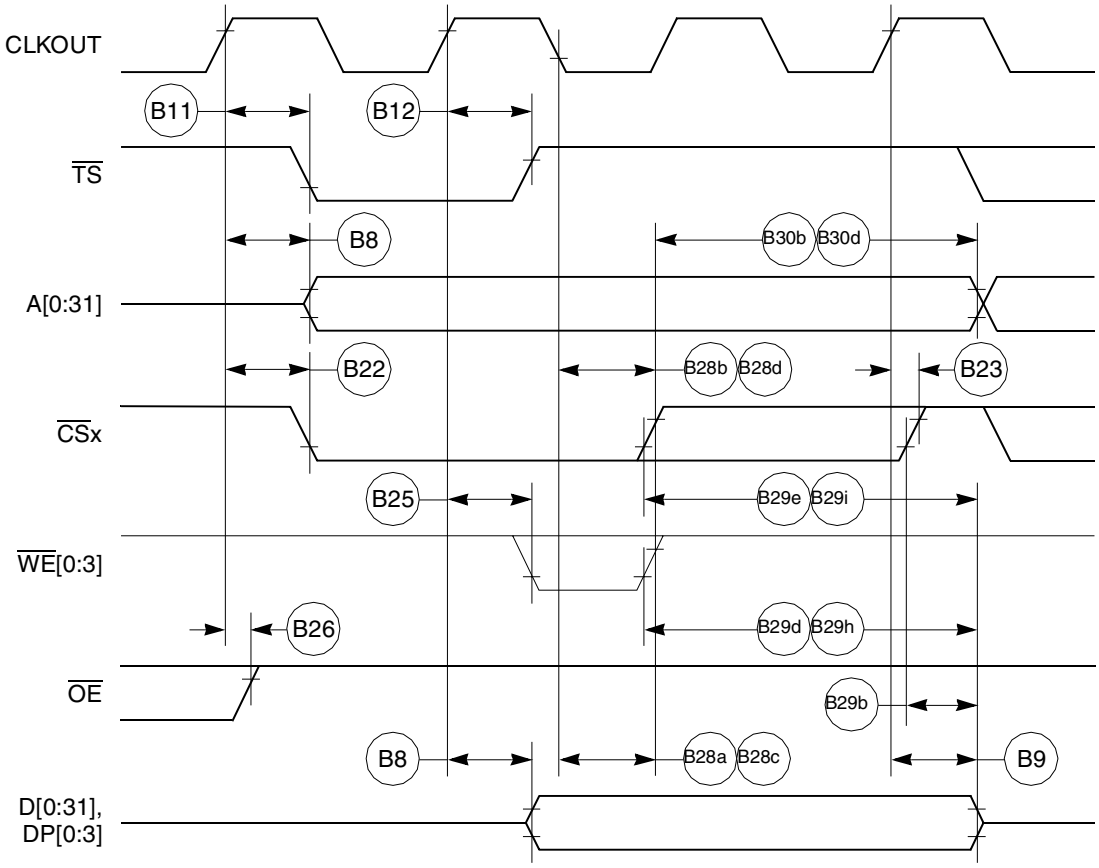


Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 1)

Figure 17 provides the timing for the external bus controlled by the UPM.

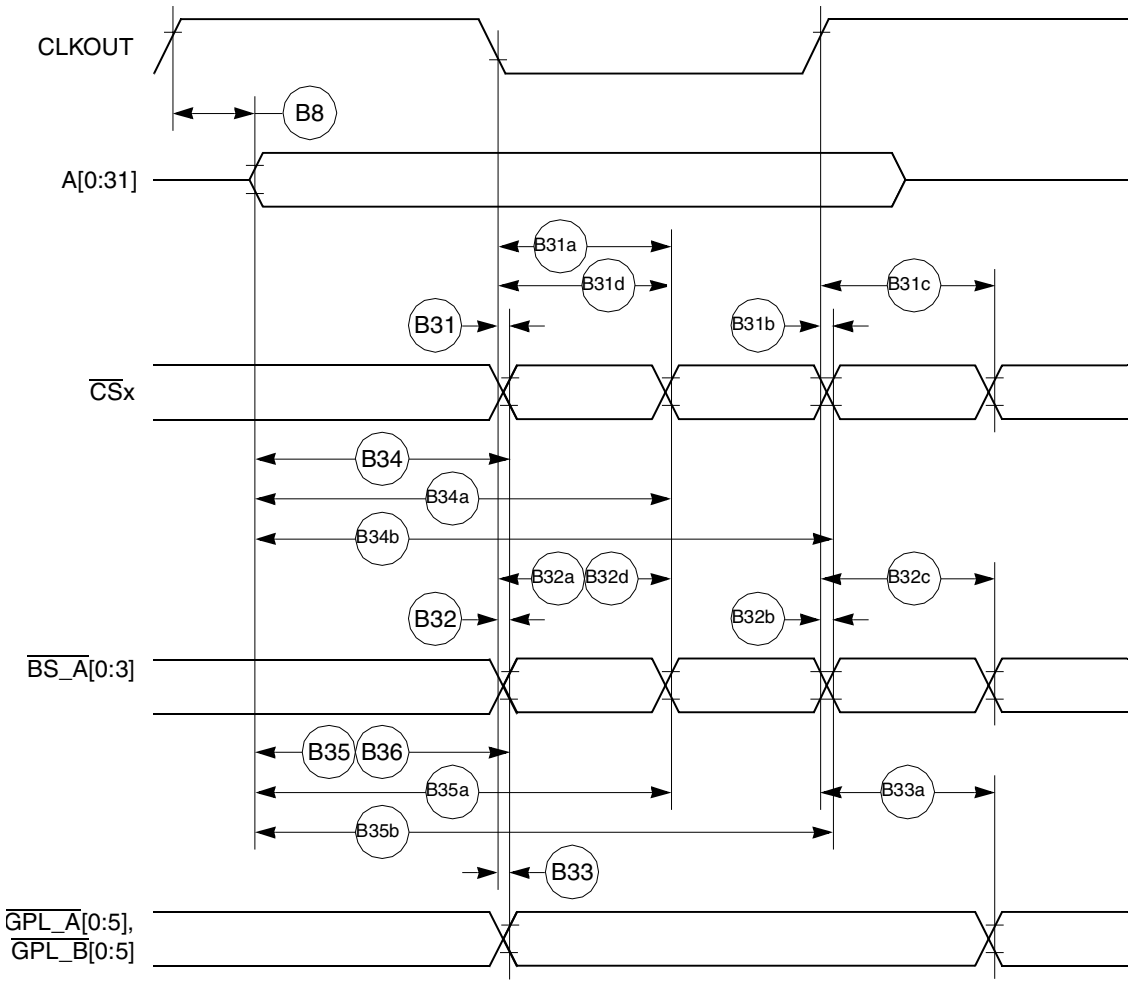


Figure 17. External Bus Timing (UPM-Controlled Signals)

Figure 18 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

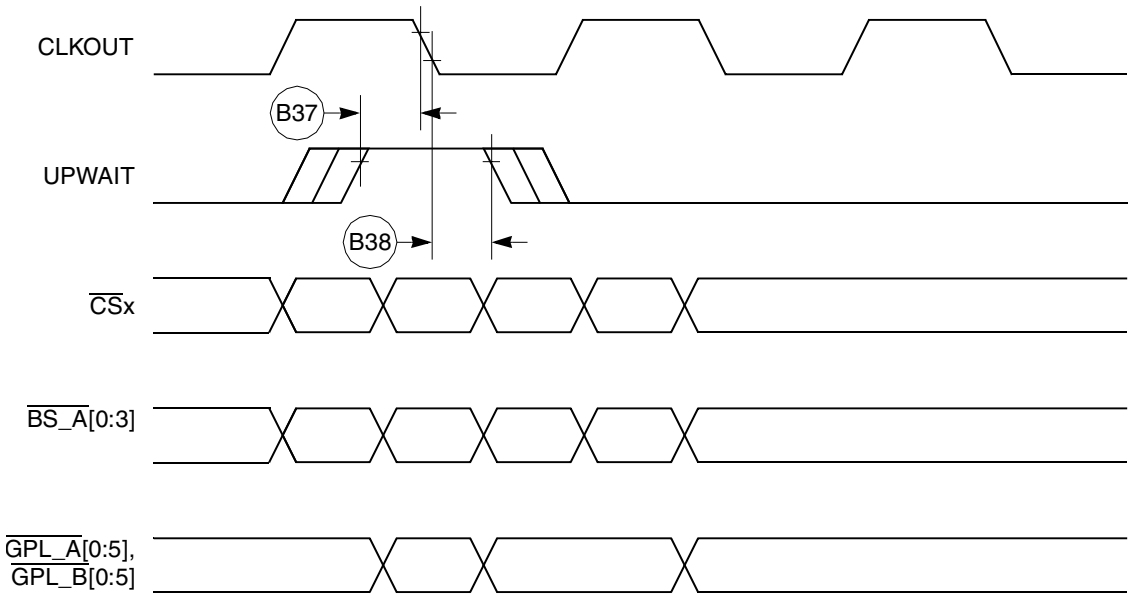


Figure 18. Asynchronous UPWAIT Asserted Detection in UPM-Handled Cycles Timing

Figure 19 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

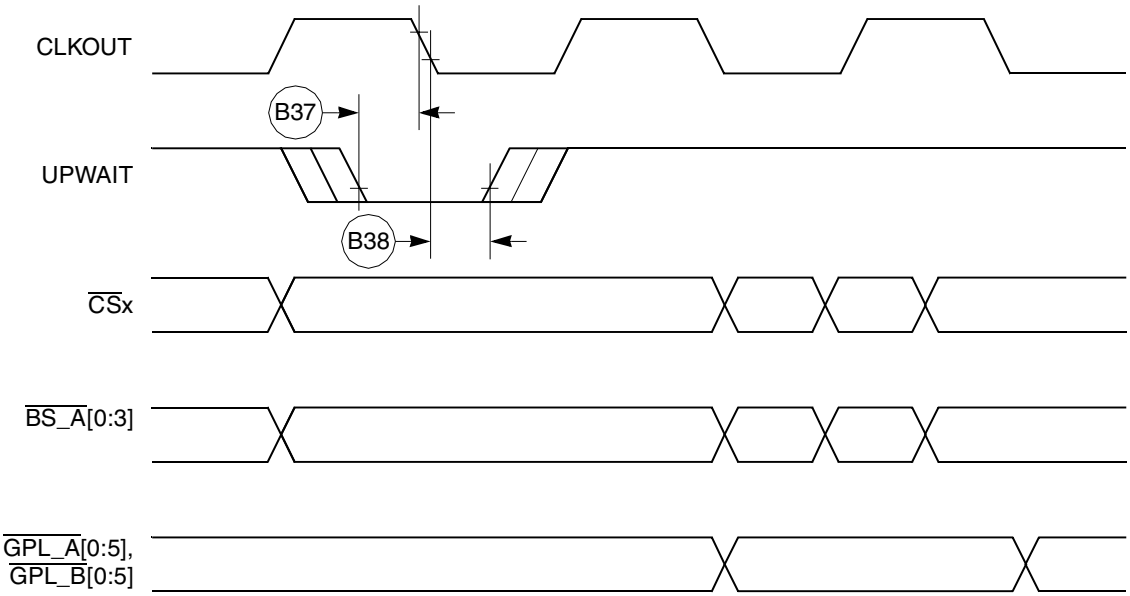


Figure 19. Asynchronous UPWAIT Negated Detection in UPM-Handled Cycles Timing

Figure 20 provides the timing for the synchronous external master access controlled by the GPCM.

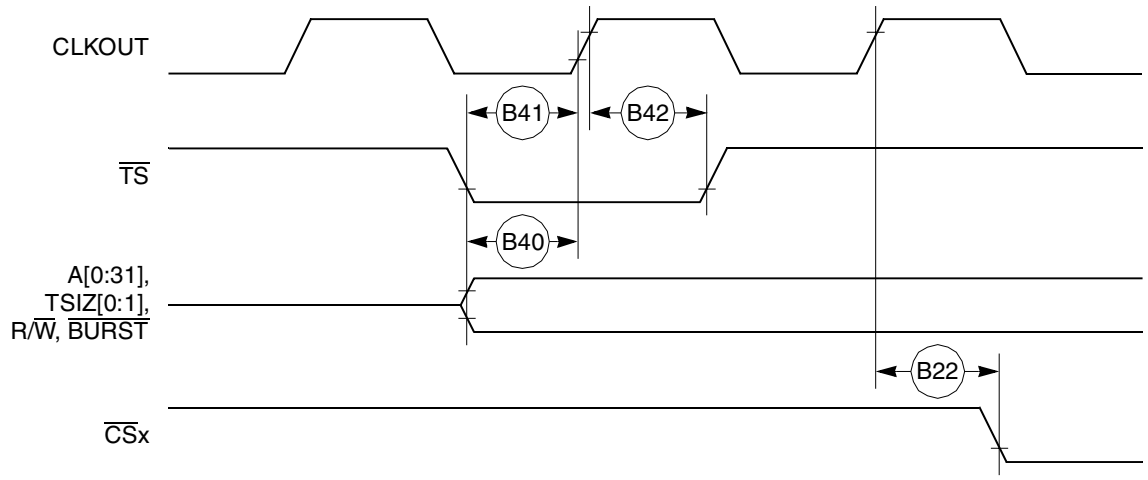


Figure 20. Synchronous External Master Access Timing (GPCM Handled—ACS = 00)

Figure 21 provides the timing for the asynchronous external master memory access controlled by the GPCM.

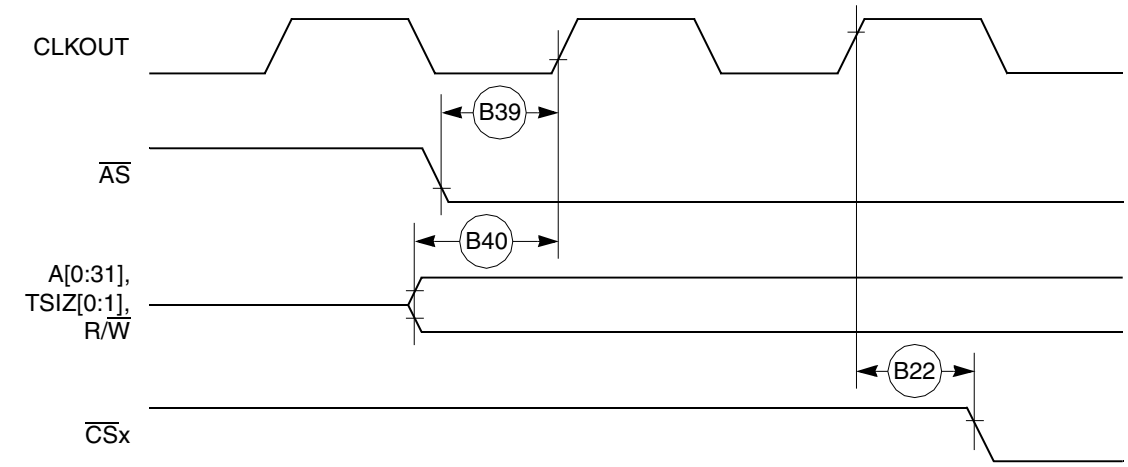


Figure 21. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 22 provides the timing for the asynchronous external master control signals negation.

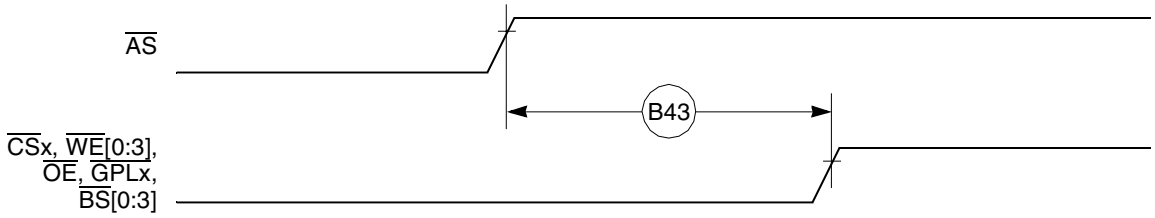


Figure 22. Asynchronous External Master—Control Signals Negation Timing

Table 10 provides interrupt timing for the MPC853T.

Table 10. Interrupt Timing

Num	Characteristic [1]	All Frequencies		Unit
		Min	Max	
I39	$\overline{\text{IRQ}}$x valid to CLKOUT rising edge (setup time)	6.00		ns
I40	$\overline{\text{IRQ}}$x hold time after CLKOUT	2.00		ns
I41	$\overline{\text{IRQ}}$x pulse width low	3.00		ns
I42	$\overline{\text{IRQ}}$x pulse width high	3.00		ns
I43	$\overline{\text{IRQ}}$x edge-to-edge time	$4 \times T_{CLOCKOUT}$		—

1 The I39 and I40 timings describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{\text{IRQ}}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC853T is able to support.

Figure 23 provides the interrupt detection timing for the external level-sensitive lines.

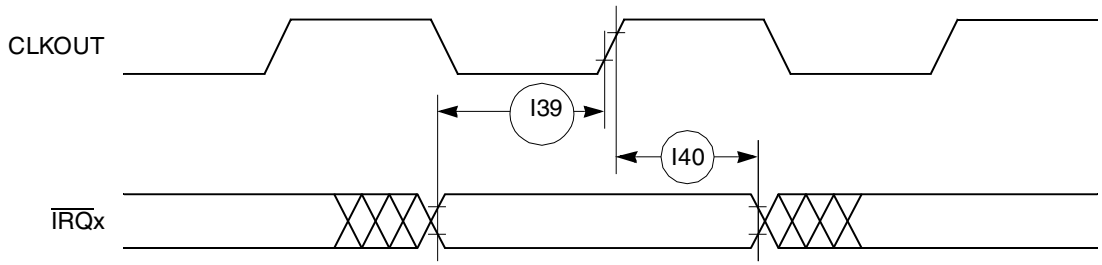


Figure 23. Interrupt Detection Timing for External Level-Sensitive Lines

Figure 24 provides the interrupt detection timing for the external edge-sensitive lines.

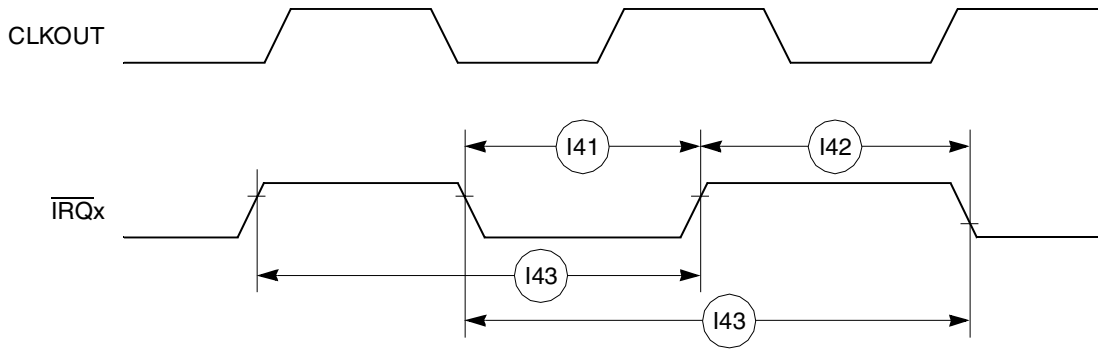


Figure 24. Interrupt Detection Timing for External Edge-Sensitive Lines

Table 11 shows the PCMCIA timing for the MPC853T.

Table 11. PCMCIA Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J82	A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted [1] (MIN = 0.75 × B1 – 2.00)	20.70	—	16.70	—	13.00	—	9.40	—	ns
J83	A(0:31), $\overline{\text{REG}}$ valid to ALE negation[1] (MIN = 1.00 × B1 – 2.00)	28.30	—	23.00	—	18.00	—	13.20	—	ns
J84	CLKOUT to $\overline{\text{REG}}$ valid (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
J85	CLKOUT to $\overline{\text{REG}}$ invalid (MIN = 0.25 × B1 + 1.00)	8.60	—	7.30	—	6.00	—	4.80	—	ns
J86	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
J87	CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated (MAX = 0.25 × B1 + 8.00)	7.60	15.60	6.30	14.30	5.00	13.00	3.80	11.80	ns
J88	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = 0.00 × B1 + 11.00)	—	11.00	—	11.00	—	11.00	—	11.00	ns
J89	CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = 0.00 × B1 + 11.00)	2.00	11.00	2.00	11.00	2.00	11.00	2.00	11.00	ns
J90	CLKOUT to ALE assert time (MAX = 0.25 × B1 + 6.30)	7.60	13.80	6.30	12.50	5.00	11.30	3.80	10.00	ns
J91	CLKOUT to ALE negate time (MAX = 0.25 × B1 + 8.00)	—	15.60	—	14.30	—	13.00	—	11.80	ns
J92	$\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1] (MIN = 0.25 × B1 – 2.00)	5.60	—	4.30	—	3.00	—	1.80	—	ns
J93	$\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] (MIN = 0.00 × B1 + 8.00)	8.00	—	8.00	—	8.00	—	8.00	—	ns
J94	CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] (MIN = 0.00 × B1 + 2.00)	2.00	—	2.00	—	2.00	—	2.00	—	ns

[1] PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITA}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITA}}$ assertion will be effective only if it is detected two cycles before the PSL timer expiration. See the Chapter 16, “PCMCIA Interface,” in the *MPC866 PowerQUICC Family User’s Manual*.

Figure 25 provides the PCMCIA access cycle timing for the external bus read.

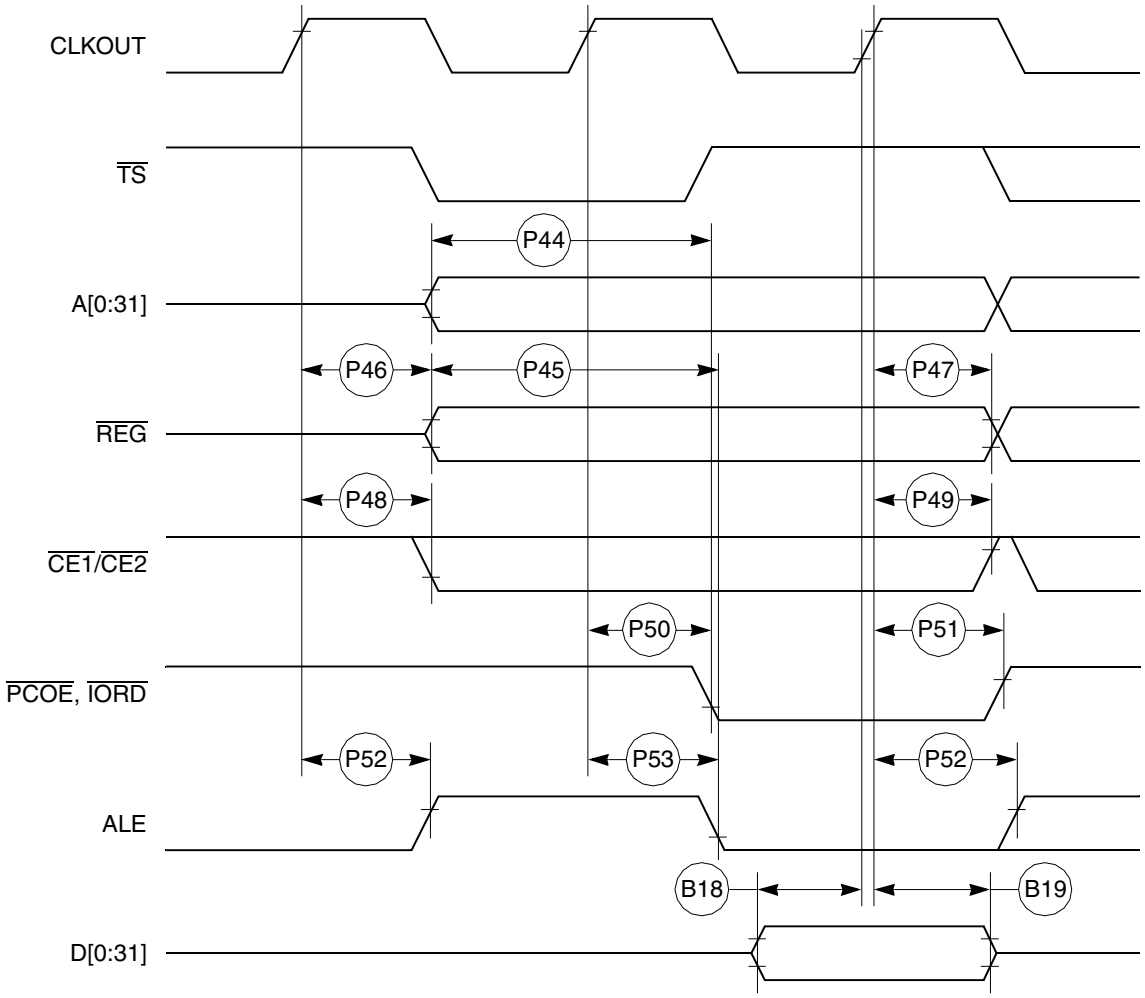


Figure 25. PCMCIA Access Cycles Timing External Bus Read

Figure 26 provides the PCMCIA access cycle timing for the external bus write.

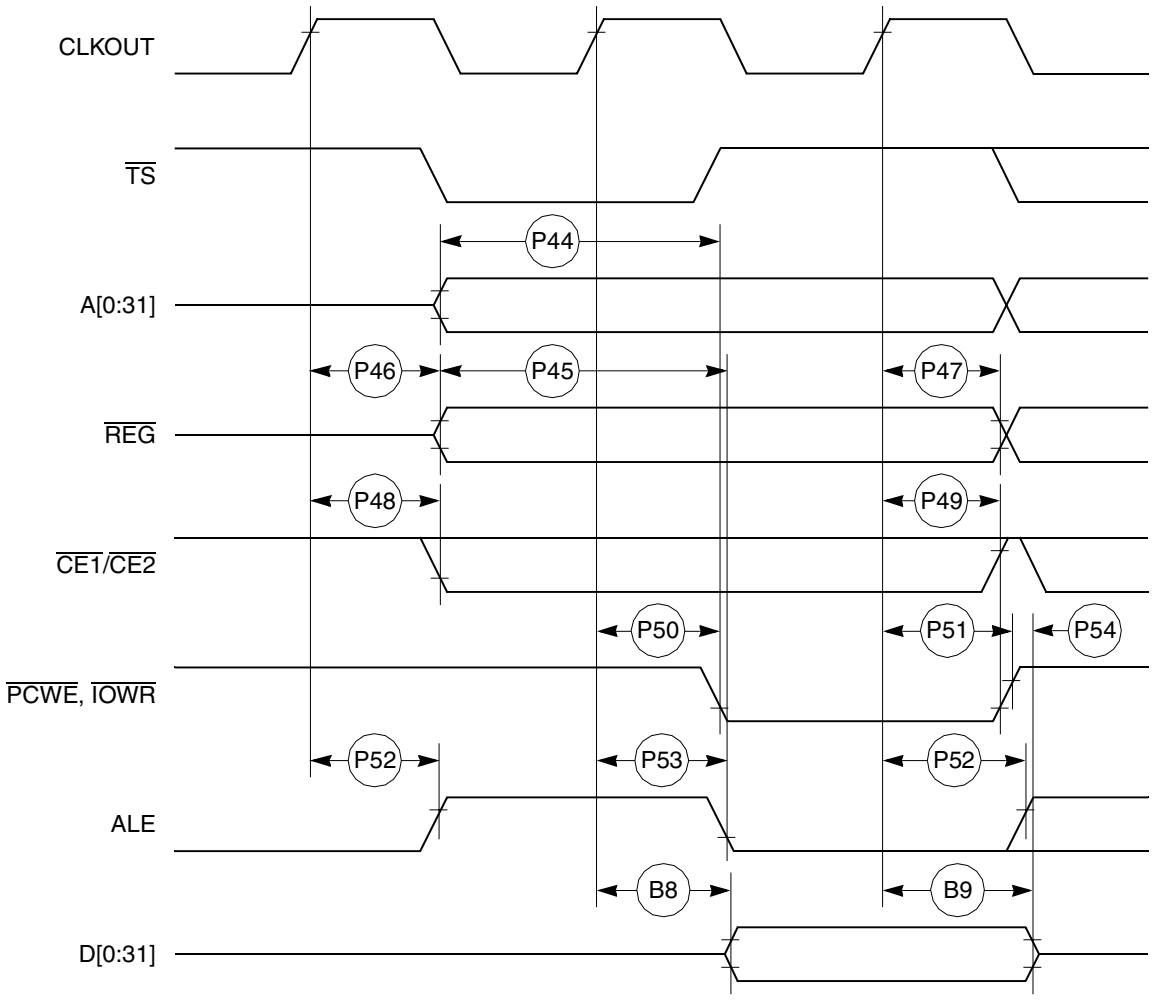


Figure 26. PCMCIA Access Cycles Timing External Bus Write

Figure 27 provides the PCMCIA WAIT signals detection timing.

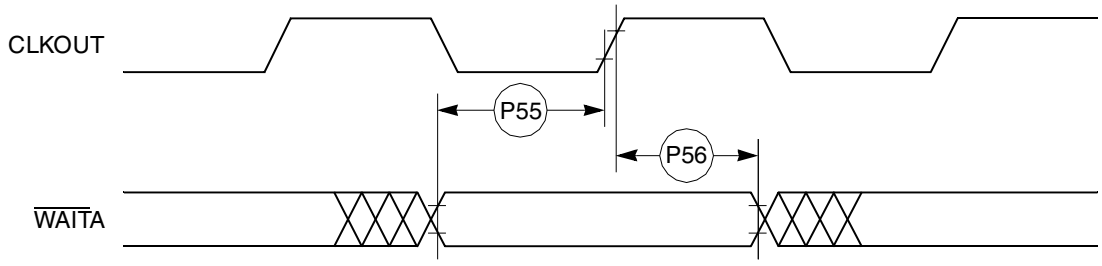


Figure 27. PCMCIA WAIT Signals Detection Timing

Table 12 shows the PCMCIA port timing for the MPC853T.

Table 12. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J95	CLKOUT to OPx valid (MAX = 0.00 × B1 + 19.00)	—	19.00	—	19.00	—	19.00	—	19.00	ns
J96	$\overline{\text{HRESET}}$ negated to OPx drive [1] (MIN = 0.75 × B1 + 3.00)	25.70	—	21.70	—	18.00	—	14.40	—	ns
J97	IP_Xx valid to CLKOUT rising edge (MIN = 0.00 × B1 + 5.00)	5.00	—	5.00	—	5.00	—	5.00	—	ns
J98	CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 × B1 + 1.00)	1.00	—	1.00	—	1.00	—	1.00	—	ns

1 OP2 and OP3 only.

Figure 28 provides the PCMCIA output port timing for the MPC853T.

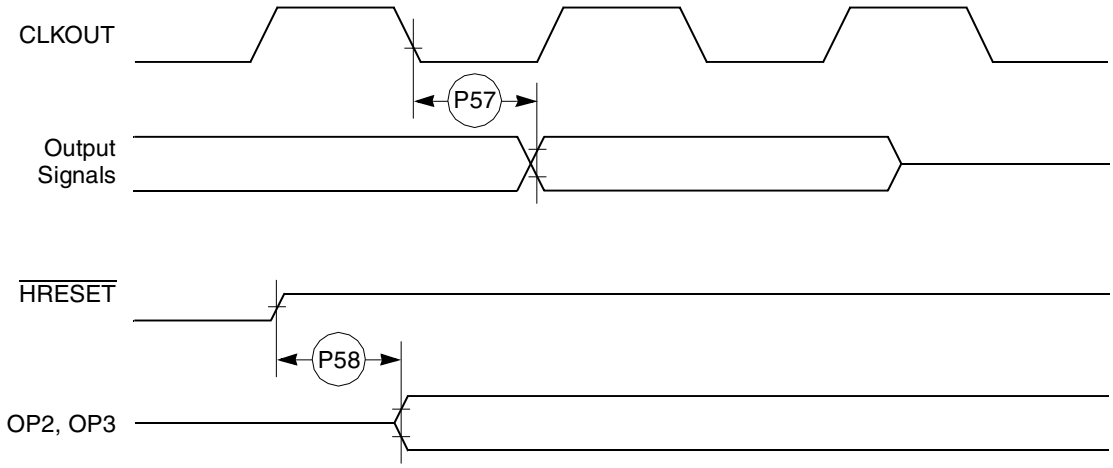


Figure 28. PCMCIA Output Port Timing

Figure 29 provides the PCMCIA in put port timing for the MPC853T.

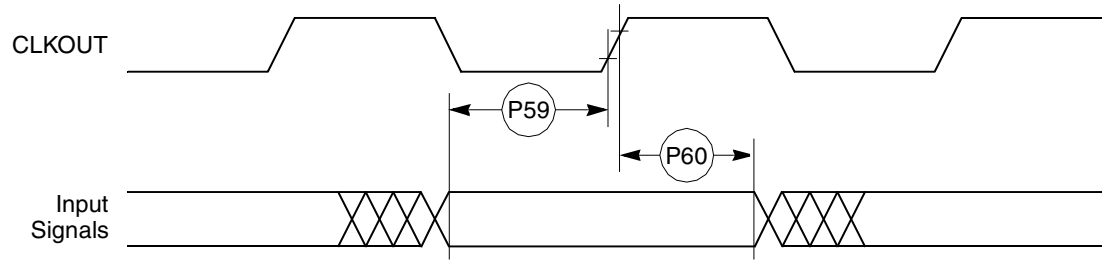


Figure 29. PCMCIA Input Port Timing

Table 13 shows the debug port timing for the MPC853T.

Table 13. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	DSCK cycle time	$3 \times T_{CLOCKOUT}$		—
J83	DSCK clock pulse width	$1.25 \times T_{CLOCKOUT}$		—
J84	DSCK rise and fall times	0.00	3.00	ns
J85	DSDI input data setup time	8.00		ns
J86	DSDI data hold time	5.00		ns
J87	DSCK low to DSDO data valid	0.00	15.00	ns
J88	DSCK low to DSDO invalid	0.00	2.00	ns

Figure 30 provides the input timing for the debug port clock.

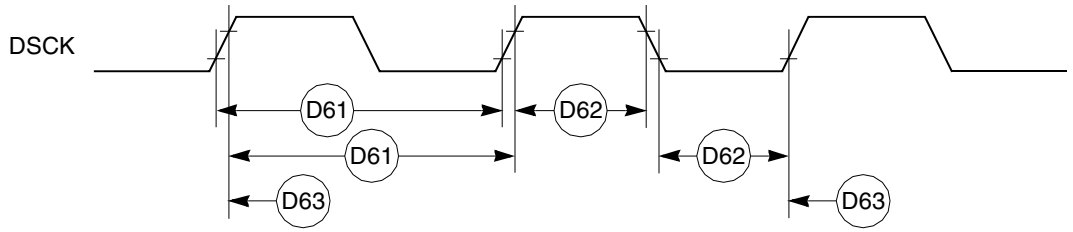


Figure 30. Debug Port Clock Input Timing

Figure 31 provides the timing for the debug port.

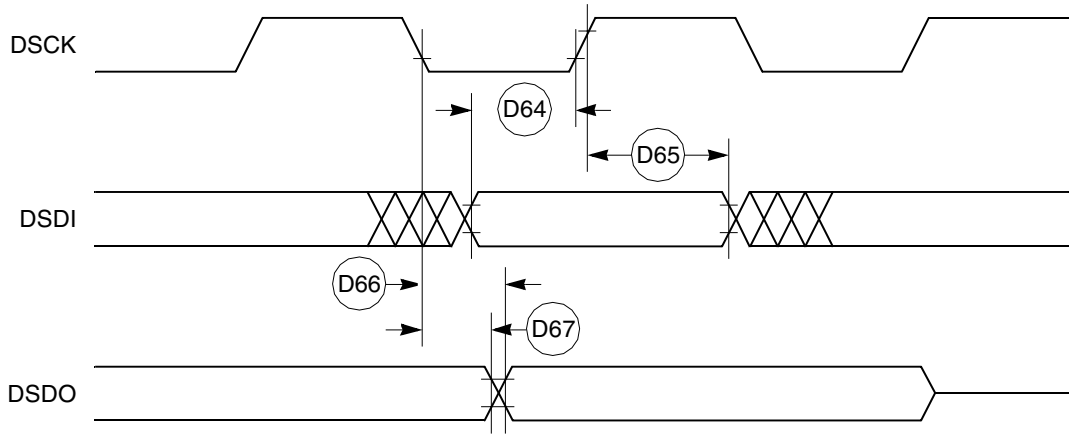


Figure 31. Debug Port Timings

Table 14 shows the reset timing for the MPC853T.

Table 14. Reset Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
J82	CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J83	CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 × B1 + 20.00)	—	20.00	—	20.00	—	20.00	—	20.00	ns
J84	$\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 × B1)	515.20	—	425.00	—	340.00	—	257.60	—	ns
J85	—	—	—	—	—	—	—	—	—	—
J86	Configuration data to HRESET rising edge setup time (MIN = 15.00 × B1 + 50.00)	504.50	—	425.00	—	350.00	—	277.30	—	ns
J87	Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 × B1 + 350.00)	350.00	—	350.00	—	350.00	—	350.00	—	ns
J88	Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J89	Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J90	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J91	$\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J92	CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 × B1 + 25.00)	—	25.00	—	25.00	—	25.00	—	25.00	ns
J93	DSDI, DSCK setup (MIN = 3.00 × B1)	90.90	—	75.00	—	60.00	—	45.50	—	ns
J94	DSDI, DSCK hold time (MIN = 0.00 × B1 + 0.00)	0.00	—	0.00	—	0.00	—	0.00	—	ns
J95	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 × B1)	242.40	—	200.00	—	160.00	—	121.20	—	ns

Figure 32 shows the reset timing for the data bus configuration.

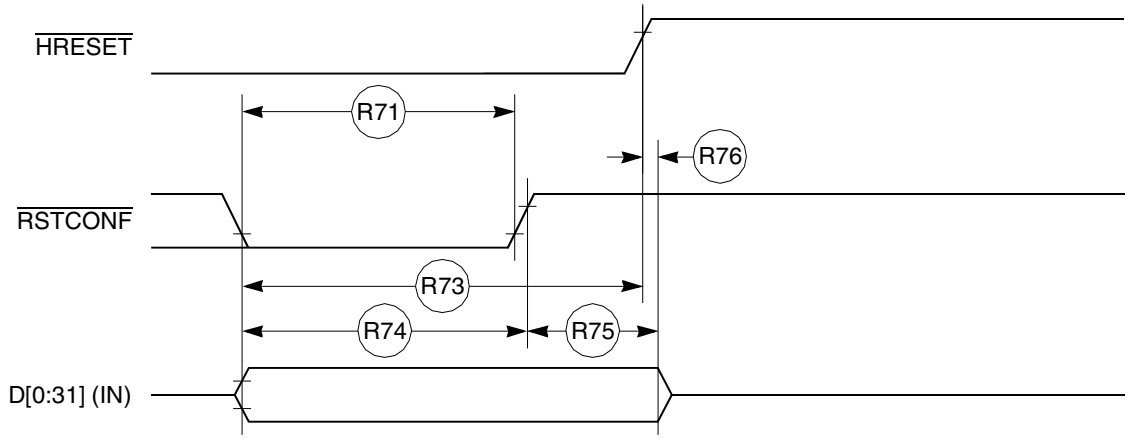


Figure 32. Reset Timing—Configuration from Data Bus

Figure 33 provides the reset timing for the data bus weak drive during configuration.

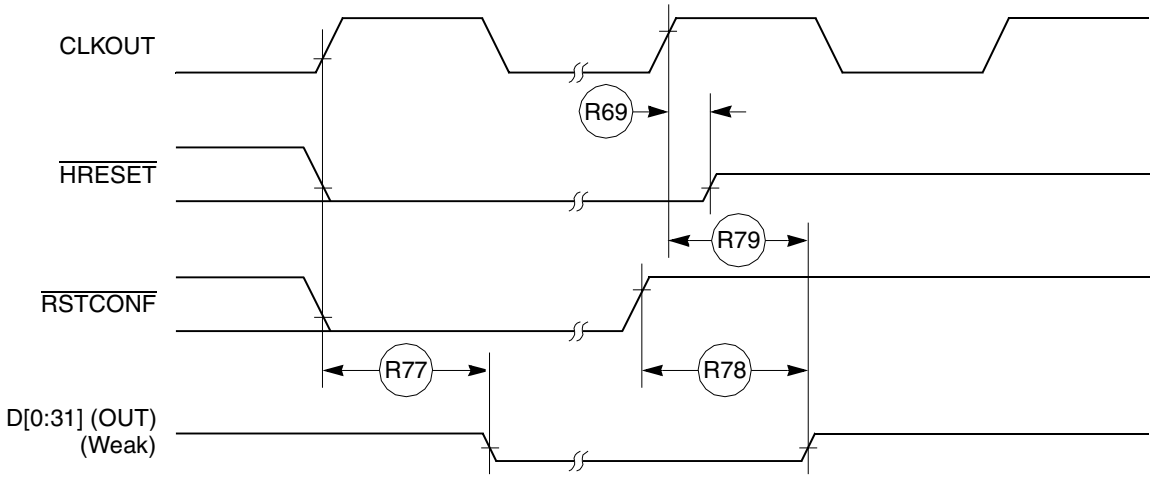


Figure 33. Reset Timing—Data Bus Weak Drive During Configuration

Figure 34 provides the reset timing for the debug port configuration.

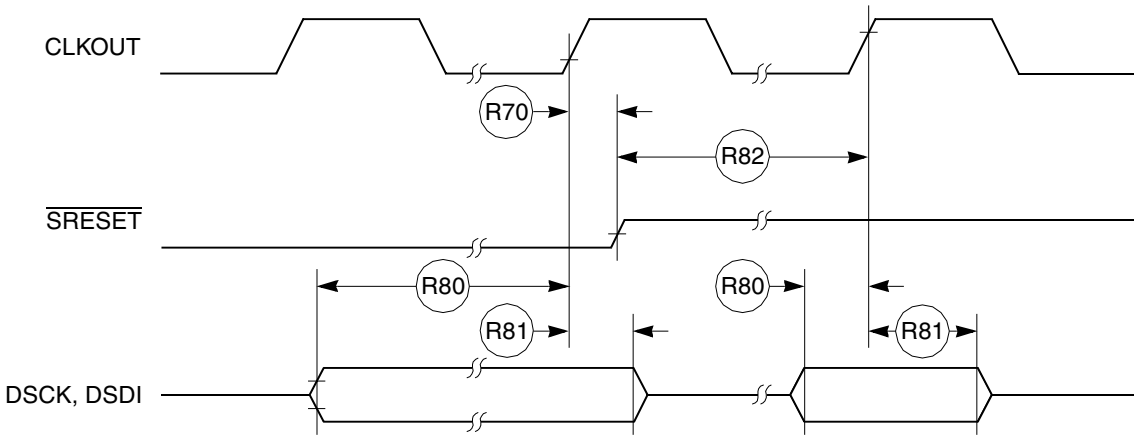


Figure 34. Reset Timing—Debug Port Configuration

12 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC853T shown in Figure 35 to Figure 38.

Table 15. JTAG Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
J82	TCK cycle time	100.00	—	ns
J83	TCK clock pulse width measured at 1.5 V	40.00	—	ns
J84	TCK rise and fall times	0.00	10.00	ns
J85	TMS, TDI data setup time	5.00	—	ns
J86	TMS, TDI data hold time	25.00	—	ns
J87	TCK low to TDO data valid	—	27.00	ns
J88	TCK low to TDO data invalid	0.00	—	ns
J89	TCK low to TDO high impedance	—	20.00	ns
J90	$\overline{\text{TRST}}$ assert time	100.00	—	ns
J91	$\overline{\text{TRST}}$ setup time to TCK low	40.00	—	ns
J92	TCK falling edge to output valid	—	50.00	ns
J93	TCK falling edge to output valid out of high impedance	—	50.00	ns
J94	TCK falling edge to output high impedance	—	50.00	ns
J95	Boundary scan input valid to TCK rising edge	50.00	—	ns
J96	TCK rising edge to boundary scan input invalid	50.00	—	ns

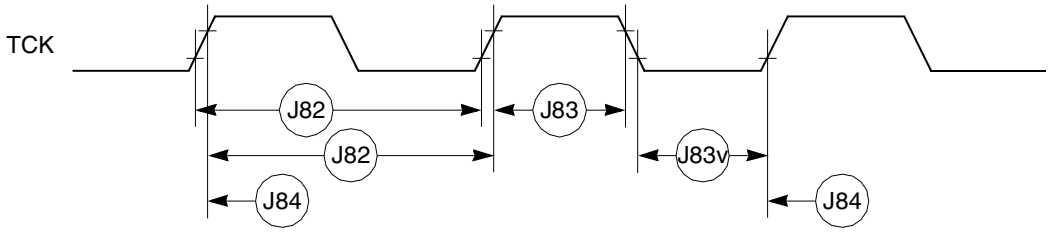


Figure 35. JTAG Test Clock Input Timing

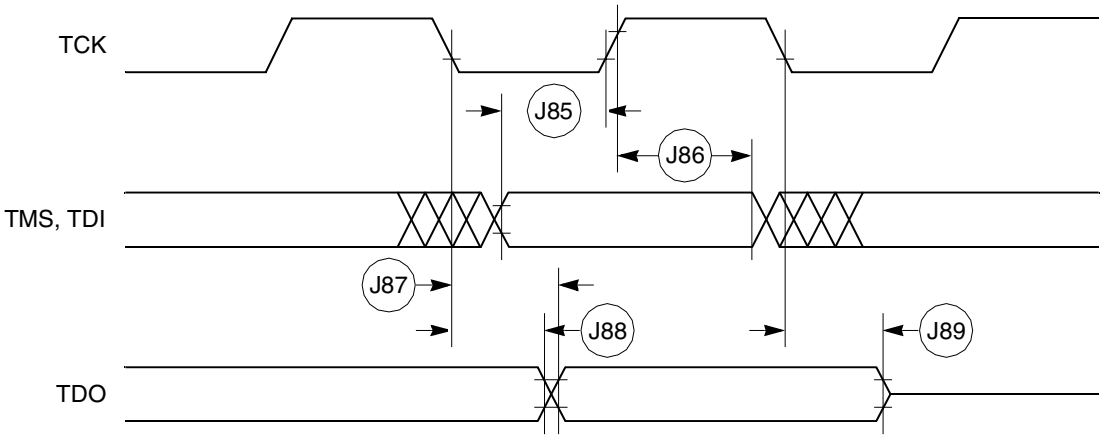


Figure 36. JTAG Test Access Port Timing Diagram

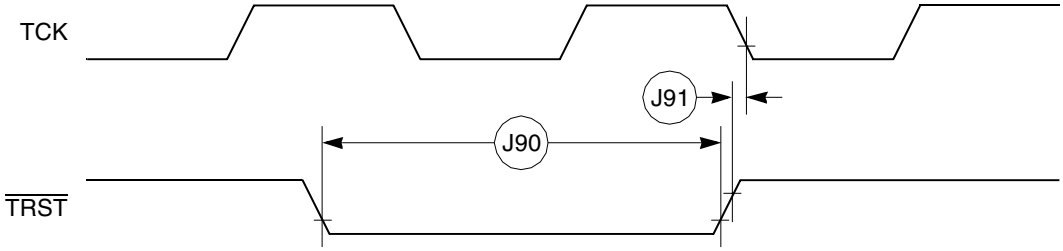


Figure 37. JTAG $\overline{\text{TRST}}$ Timing Diagram

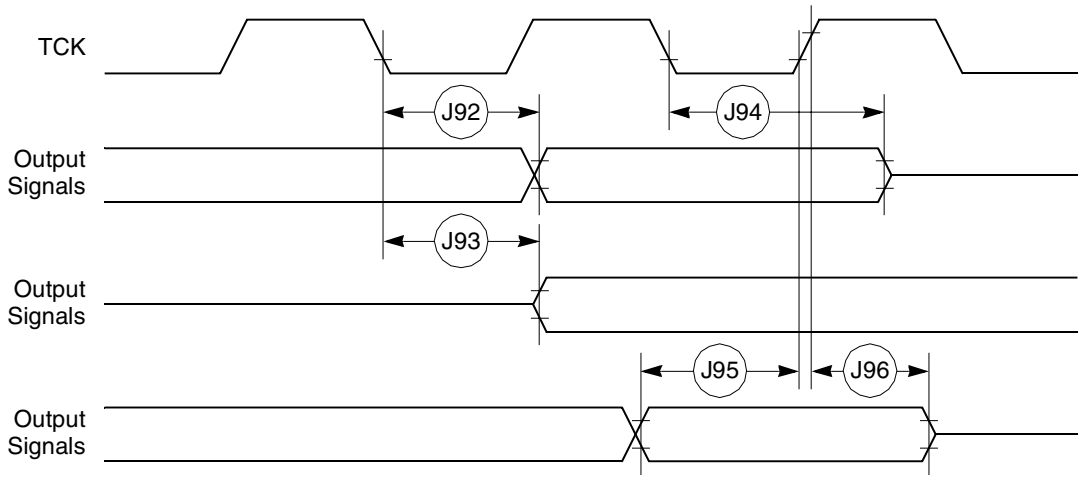


Figure 38. Boundary Scan (JTAG) Timing Diagram

13 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC853T.

13.1 Port C Interrupt AC Electrical Specifications

Table 16 provides the timings for port C interrupts.

Table 16. Port C Interrupt Timing

Num	Characteristic	33.34 MHz		Unit
		Min	Max	
35	Port C interrupt pulse width low (edge-triggered mode)	55	—	ns
36	Port C interrupt minimum time between active edges	55	—	ns

Figure 39 shows the port C interrupt detection timing.

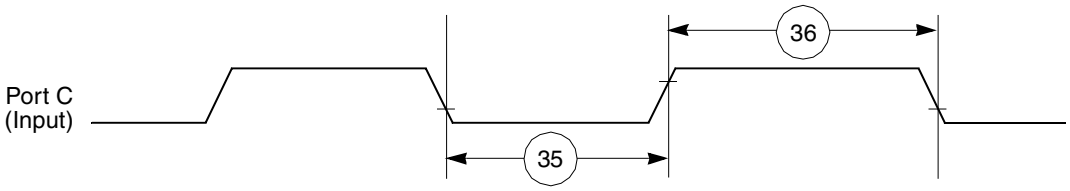


Figure 39. Port C Interrupt Detection Timing

13.2 IDMA Controller AC Electrical Specifications

Table 17 provides the IDMA controller timings as shown in Figure 40 to Figure 43.

Table 17. IDMA Controller Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
40	$\overline{\text{DREQ}}$ setup time to clock high	7	—	ns
41	$\overline{\text{DREQ}}$ hold time from clock high [1]	3	—	ns
42	$\overline{\text{SDACK}}$ assertion delay from clock high	—	12	ns
43	$\overline{\text{SDACK}}$ negation delay from clock low	—	12	ns
44	$\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low	—	20	ns
45	$\overline{\text{SDACK}}$ negation delay from clock high	—	15	ns
46	$\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$)	7	—	ns

1 Applies to high-to-low mode (EDM=1)

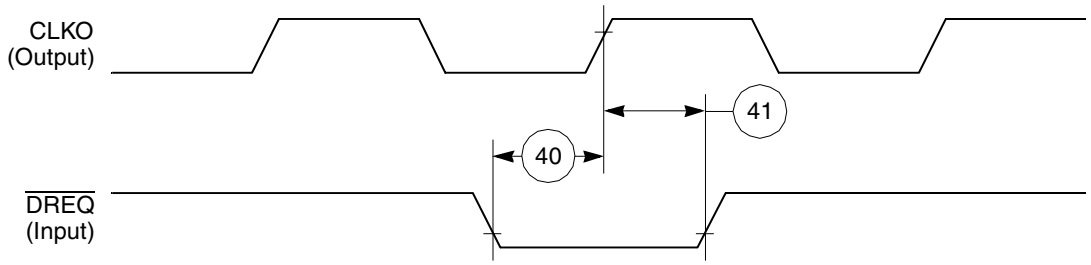


Figure 40. IDMA External Requests Timing Diagram

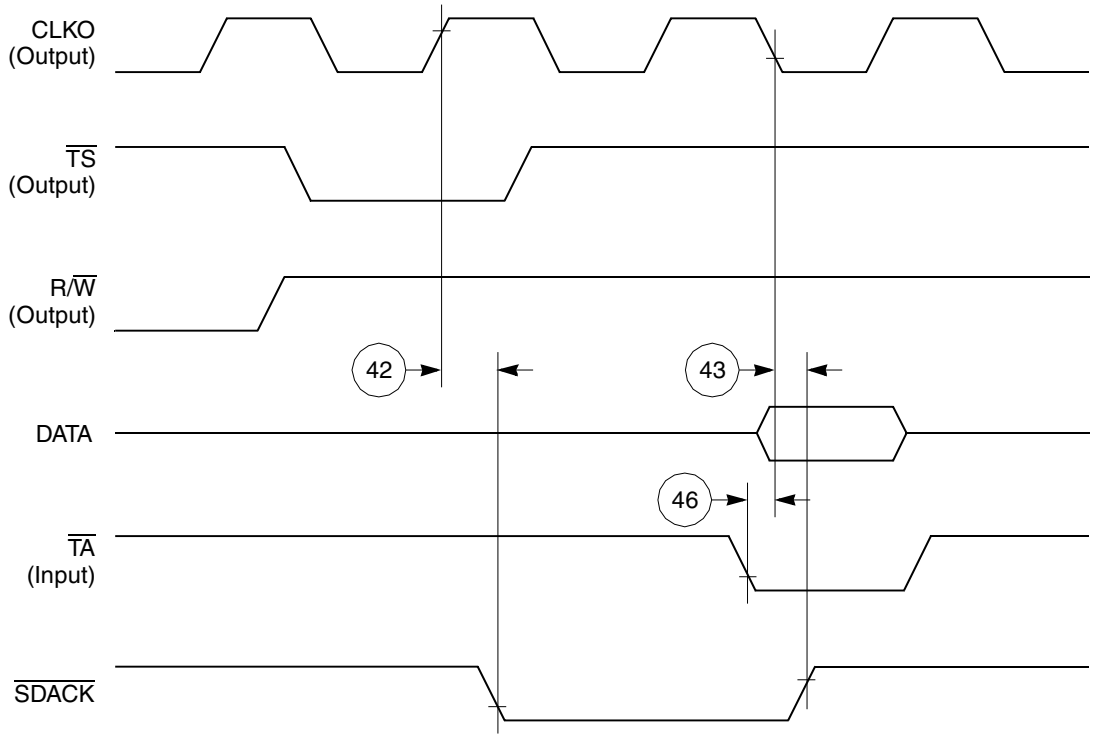


Figure 41. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA

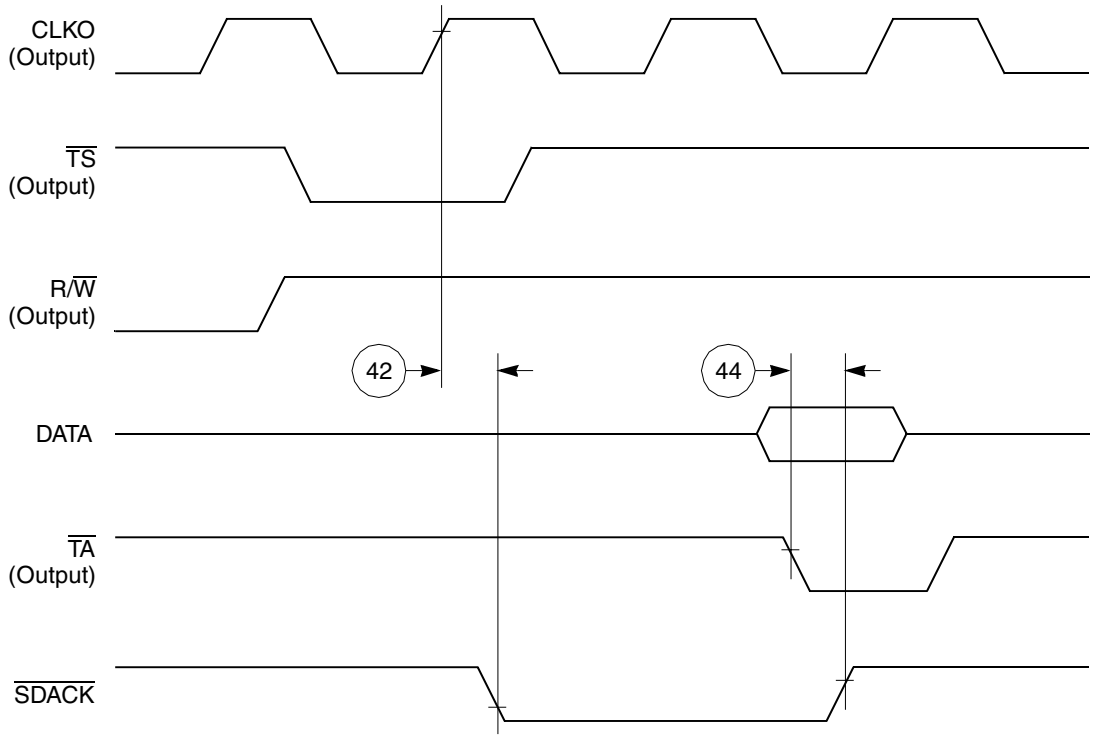


Figure 42. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA

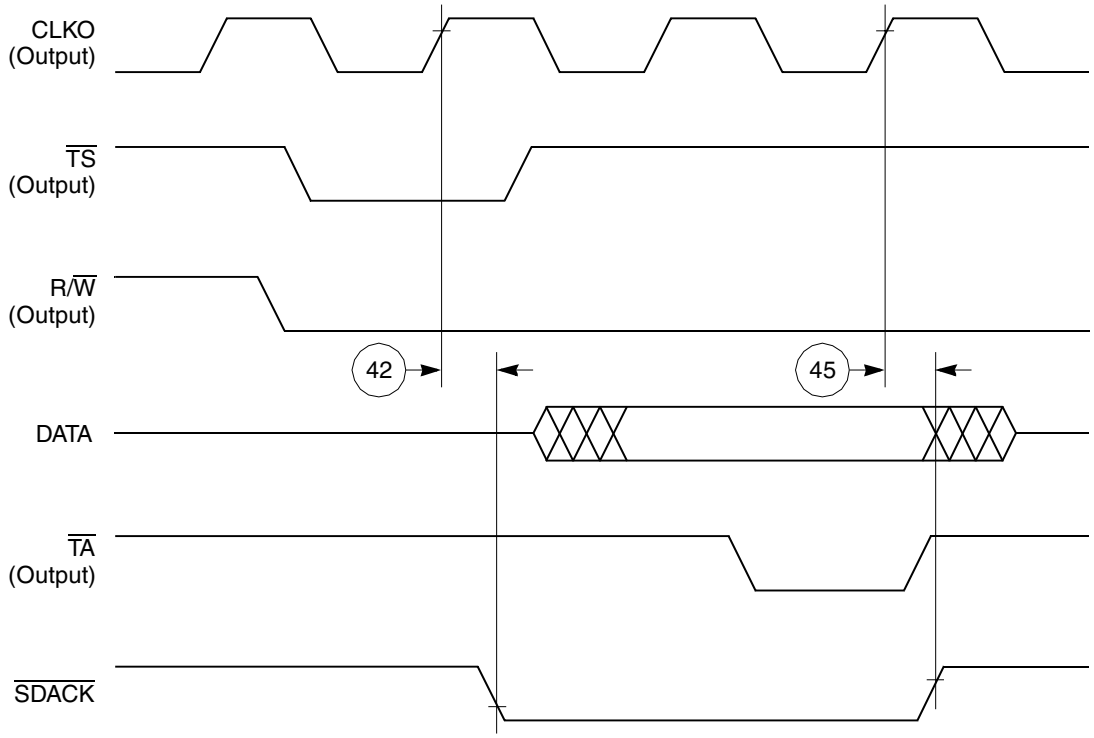


Figure 43. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA

13.3 Baud-Rate Generator AC Electrical Specifications

Table 18 provides the baud-rate generator timings as shown in Figure 44.

Table 18. Baud Rate Generator Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
50	BRGO rise and fall time	—	10	ns
51	BRGO duty cycle	40	60	%
52	BRGO cycle	40	—	ns

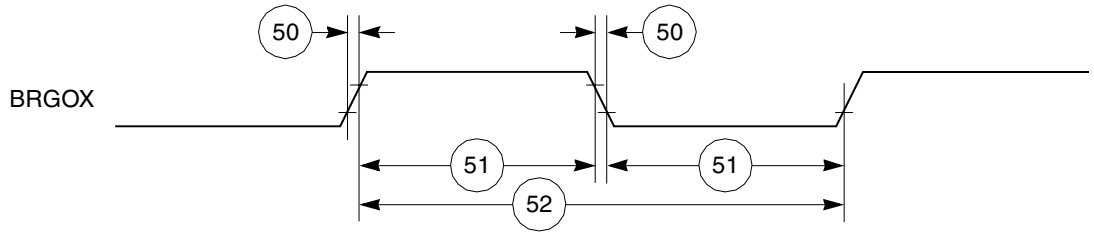


Figure 44. Baud Rate Generator Timing Diagram

13.4 Timer AC Electrical Specifications

Table 19 provides the general-purpose timer timings as shown in Figure 45.

Table 19. Timer Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
61	TIN/$\overline{\text{TGATE}}$ rise and fall time	10	—	ns
62	TIN/$\overline{\text{TGATE}}$ low time	1	—	CLK
63	TIN/$\overline{\text{TGATE}}$ high time	2	—	CLK
64	TIN/$\overline{\text{TGATE}}$ cycle time	3	—	CLK
65	CLKO low to $\overline{\text{TOUT}}$ valid	3	25	ns

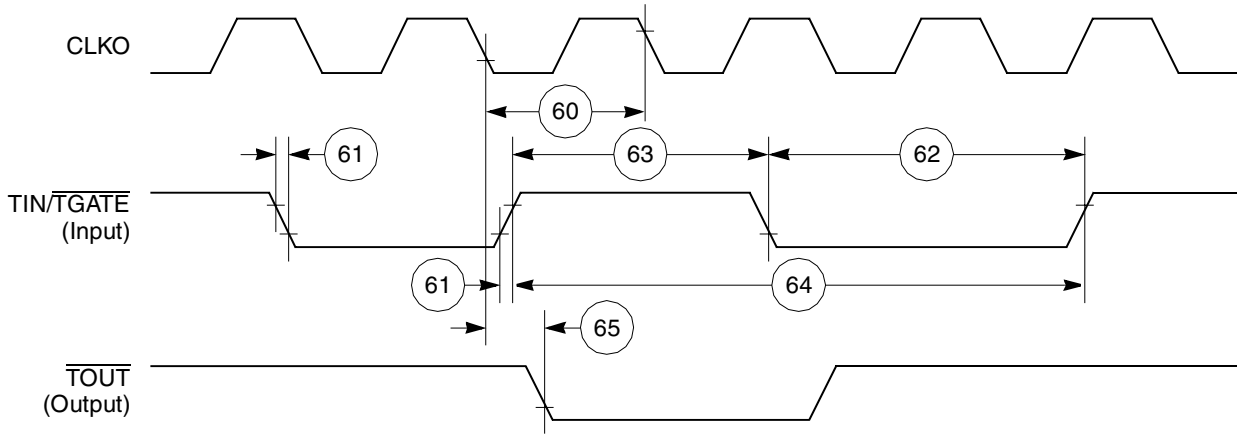


Figure 45. CPM General-Purpose Timers Timing Diagram

13.5 Serial Interface AC Electrical Specifications

Table 20 provides the serial interface (SI) timings as shown in Figure 46 to Figure 50.

Table 20. SI Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
70	L1RCLKB, L1TCLKB frequency (DSC = 0) [1, 2]	—	SYNCCLK/2 .5	MHz
71	L1RCLKB, L1TCLKB width low (DSC = 0) [2]	P + 10	—	ns
71a	L1RCLKB, L1TCLKB width high (DSC = 0) [3]	P + 10	—	ns
72	L1TXDB, L1ST1 and L1ST2, $\overline{\text{L1RQ}}$, L1CLKO rise/fall time	—	15.00	ns
73	L1RSYNCB, L1TSYNCB valid to L1CLKB edge (SYNC setup time)	20.00	—	ns
74	L1CLKB edge to L1RSYNCB, L1TSYNCB, invalid (SYNC hold time)	35.00	—	ns

Table 20. SI Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
75	L1RSYNCB, L1TSYNCB rise/fall time	—	15.00	ns
76	L1RXDB valid to L1CLKB edge (L1RXDB setup time)	17.00	—	ns
77	L1CLKB edge to L1RXDB invalid (L1RXDB hold time)	13.00	—	ns
78	L1CLKB edge to L1ST1 and L1ST2 valid [4]	10.00	45.00	ns
78A	L1SYNCB valid to L1ST1 and L1ST2 valid	10.00	45.00	ns
79	L1CLKB edge to L1ST1 and L1ST2 invalid	10.00	45.00	ns
80	L1CLKB edge to L1TXDB valid	10.00	55.00	ns
80A	L1TSYNCB valid to L1TXDB valid [4]	10.00	55.00	ns
81	L1CLKB edge to L1TXDB high impedance	0.00	42.00	ns
82	L1RCLKB, L1TCLKB frequency (DSC =1)	—	16.00 or SYNCCLK/2	MHz
83	L1RCLKB, L1TCLKB width low (DSC =1)	P + 10	—	ns
83a	L1RCLKB, L1TCLKB width high (DSC = 1)[3]	P + 10	—	ns
84	L1CLKB edge to L1CLKOB valid (DSC = 1)	—	30.00	ns
85	$\overline{\text{L1RQB}}$ valid before falling edge of L1TSYNCB[4]	1.00	—	L1TCLK
86	L1GRB setup time[2]	42.00	—	ns
87	L1GRB hold time	42.00	—	ns
88	L1CLKB edge to L1SYNCB valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0)	—	0.00	ns

1 The ratio SyncCLK/L1RCLKB must be greater than 2.5/1.

2 These specs are valid for IDL mode only.

3 Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

4 These strobes and TxD on the first bit of the frame become valid after L1CLKB edge or L1SYNCB, whichever comes later.

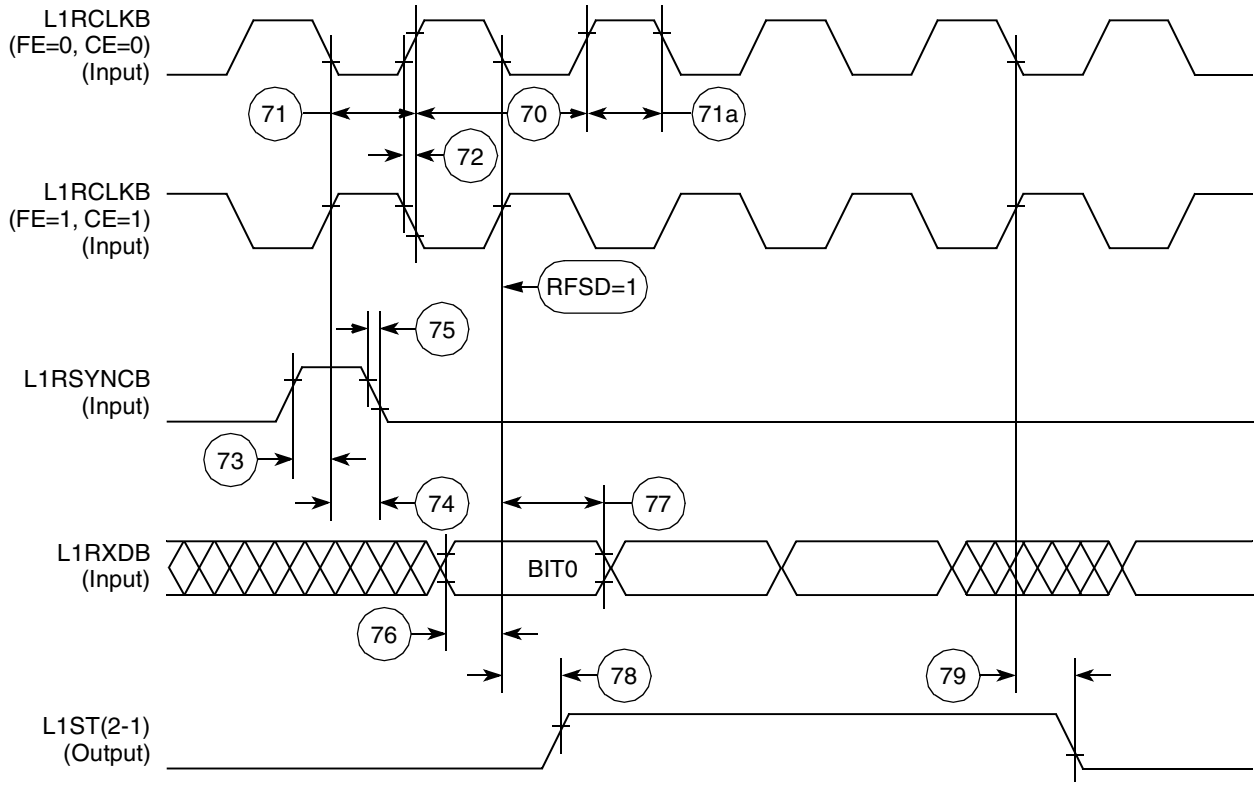


Figure 46. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

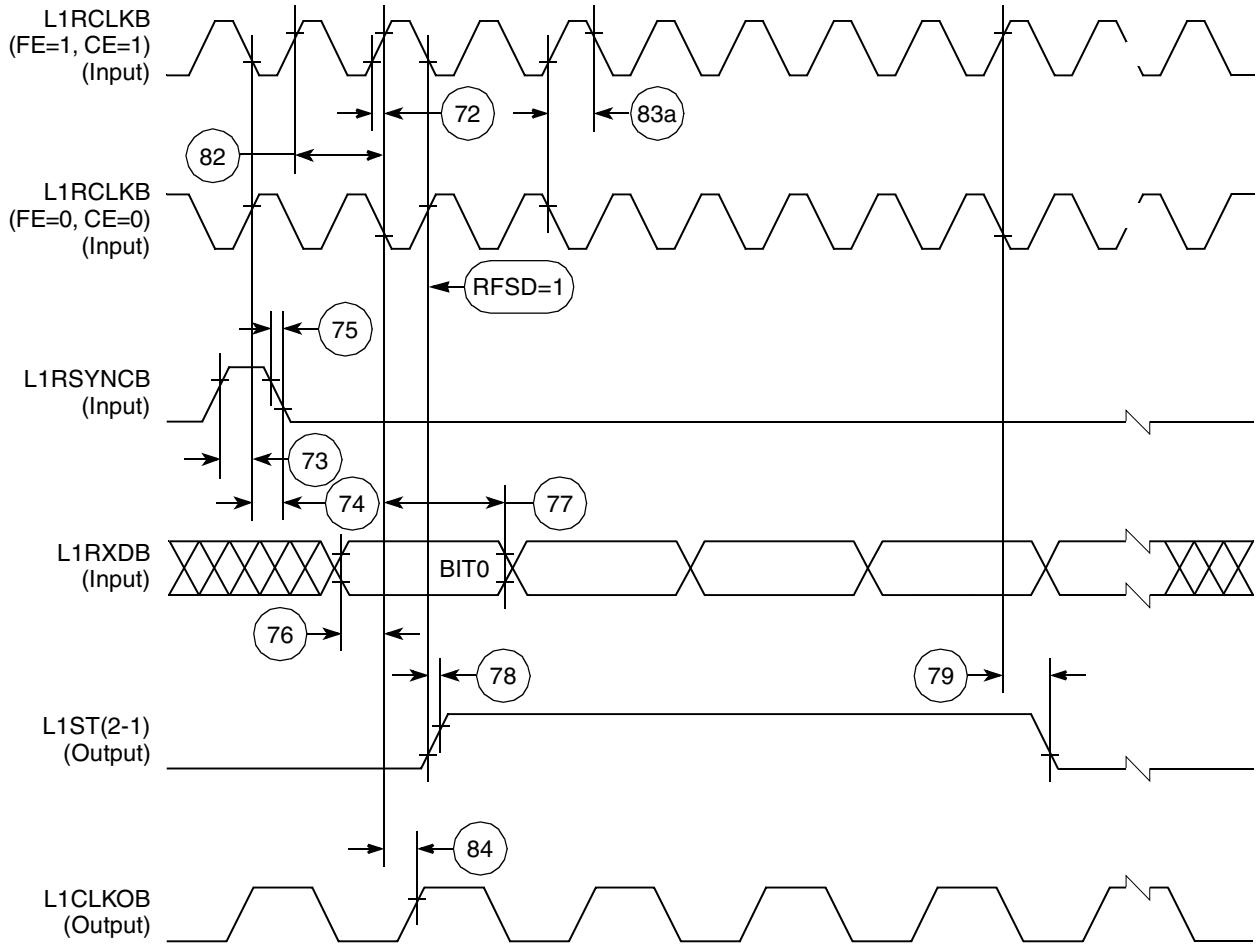


Figure 47. SI Receive Timing with Double-Speed Clocking (DSC = 1)

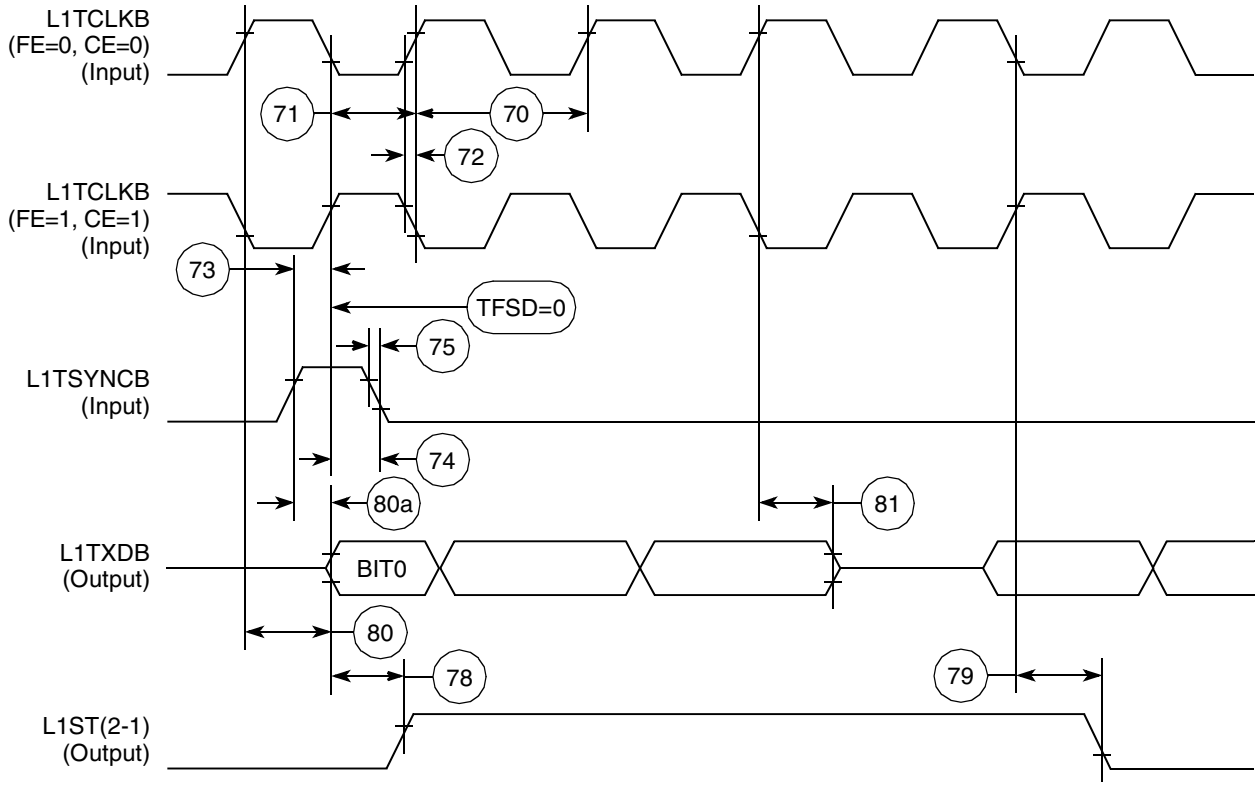


Figure 48. SI Transmit Timing Diagram (DSC = 0)

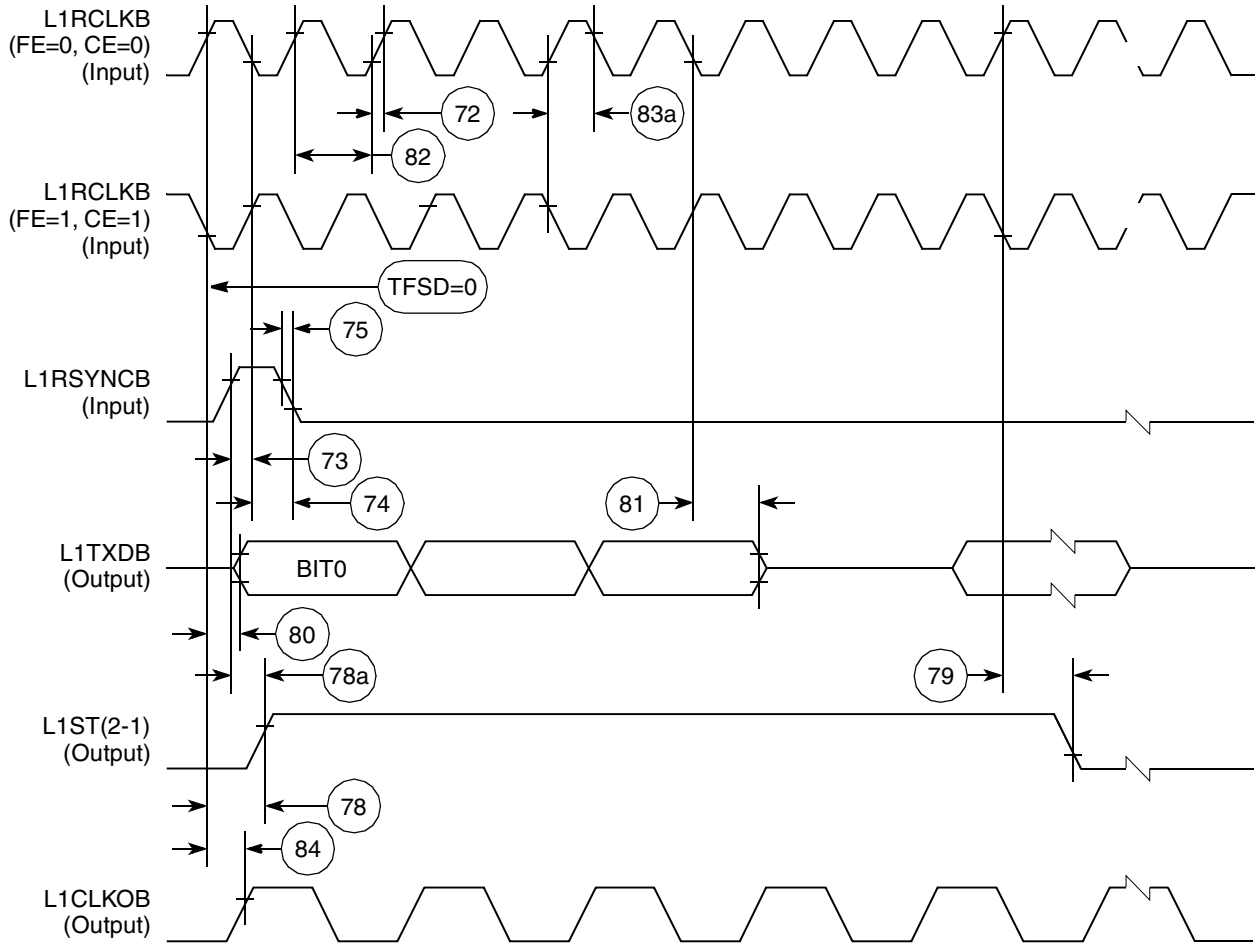


Figure 49. SI Transmit Timing with Double Speed Clocking (DSC = 1)

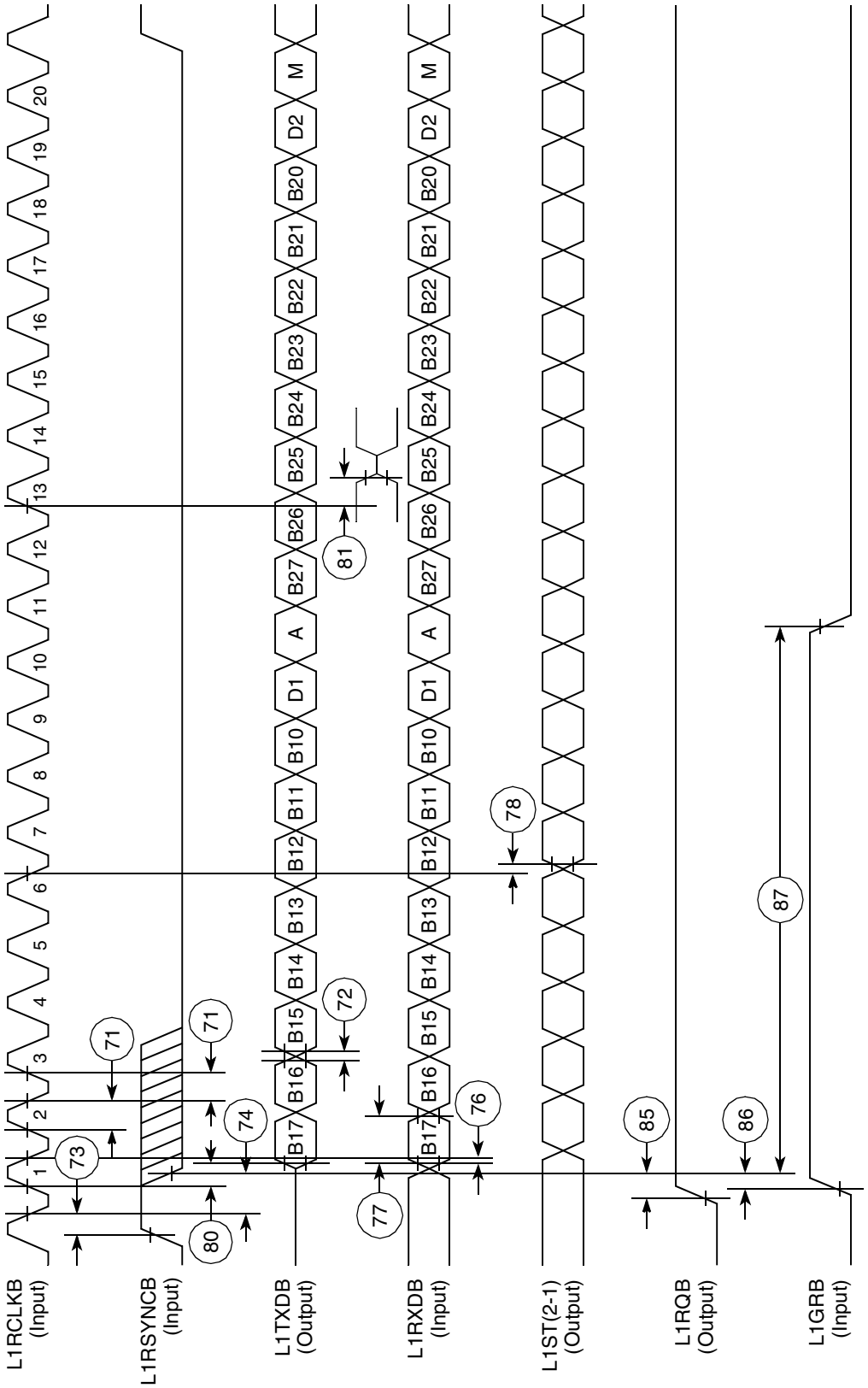


Figure 50. IDL Timing

13.6 SCC in NMSI Mode Electrical Specifications

Table 21 provides the NMSI external clock timing.

Table 21. NMSI External Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 width high [1]	1/SYNCCLK	—	ns
101	RCLK3 and TCLK3 width low	1/SYNCCLK +5	—	ns
102	RCLK3 and TCLK3 rise/fall time	—	15.00	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	50.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	50.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	5.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	5.00	—	ns
107	RXD3 hold time from RCLK3 rising edge [2]	5.00	—	ns
108	$\overline{\text{CD3}}$ setup Time to RCLK3 rising edge	5.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Table 22 provides the NMSI internal clock timing.

Table 22. NMSI Internal Clock Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
100	RCLK3 and TCLK3 frequency [1]	0.00	SYNCCLK/3	MHz
102	RCLK3 and TCLK3 rise/fall time	—	—	ns
103	TXD3 active delay (from TCLK3 falling edge)	0.00	30.00	ns
104	$\overline{\text{RTS3}}$ active/inactive delay (from TCLK3 falling edge)	0.00	30.00	ns
105	$\overline{\text{CTS3}}$ setup time to TCLK3 rising edge	40.00	—	ns
106	RXD3 setup time to RCLK3 rising edge	40.00	—	ns
107	RXD3 hold time from RCLK3 rising edge [2]	0.00	—	ns
108	$\overline{\text{CD3}}$ setup time to RCLK3 rising edge	40.00	—	ns

1 The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as external sync signals.

Figure 51 through Figure 53 show the NMSI timings.

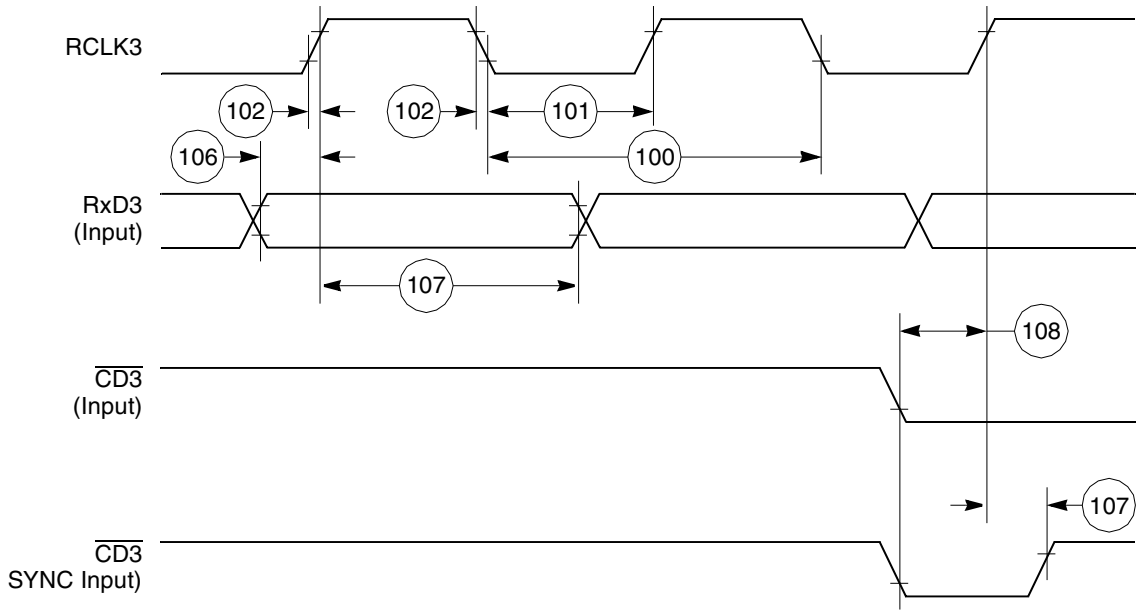


Figure 51. SCC NMSI Receive Timing Diagram

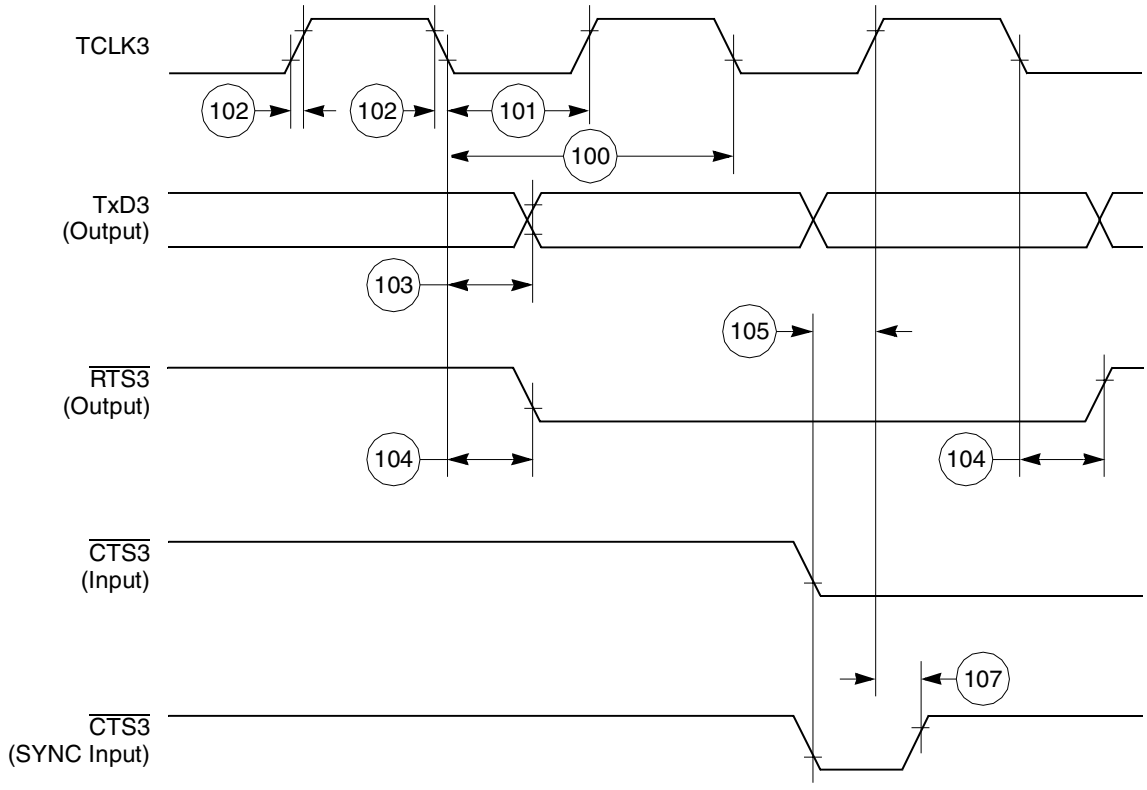


Figure 52. SCC NMSI Transmit Timing Diagram

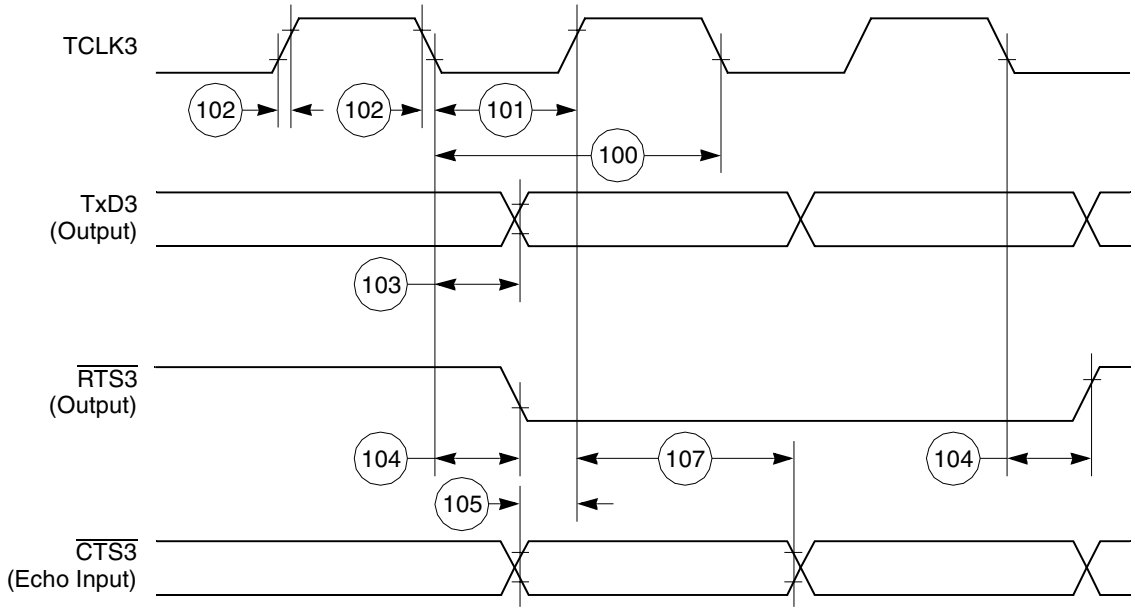


Figure 53. HDLC Bus Timing Diagram

13.7 Ethernet Electrical Specifications

Table 23 provides the Ethernet timings as shown in Figure 54 to Figure 58.

Table 23. Ethernet Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN width high	40	—	ns
121	RCLK3 rise/fall time	—	15	ns
122	RCLK3 width low	40	—	ns
123	RCLK3 clock period [1]	80	120	ns
124	RXD3 setup time	20	—	ns
125	RXD3 hold time	5	—	ns
126	RENA active delay (from RCLK3 rising edge of the last data bit)	10	—	ns
127	RENA width low	100	—	ns
128	TCLK3 rise/fall time	—	15	ns
129	TCLK3 width low	40	—	ns
130	TCLK3 clock period[1]	99	101	ns
131	TXD3 active delay (from TCLK3 rising edge)	—	50	ns
132	TXD3 inactive delay (from TCLK3 rising edge)	6.5	50	ns
133	TENA active delay (from TCLK3 rising edge)	10	50	ns

Table 23. Ethernet Timing (continued)

Num	Characteristic	All Frequencies		Unit
		Min	Max	
134	TENA inactive delay (from TCLK3 rising edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ active delay (from TCLK3 falling edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ inactive delay (from TCLK3 falling edge)	10	50	ns
137	$\overline{\text{REJECT}}$ width low	1	—	CLK
138	CLKO1 low to $\overline{\text{SDACK}}$ asserted [2]	—	20	ns
139	CLKO1 low to $\overline{\text{SDACK}}$ negated [2]	—	20	ns

[1] The ratios SyncCLK/RCLK3 and SyncCLK/TCLK3 must be greater than or equal to 2/1.

[2] $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

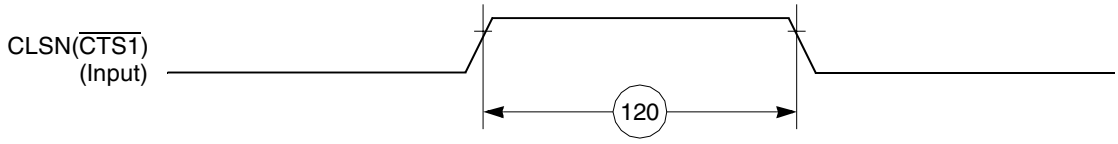


Figure 54. Ethernet Collision Timing Diagram

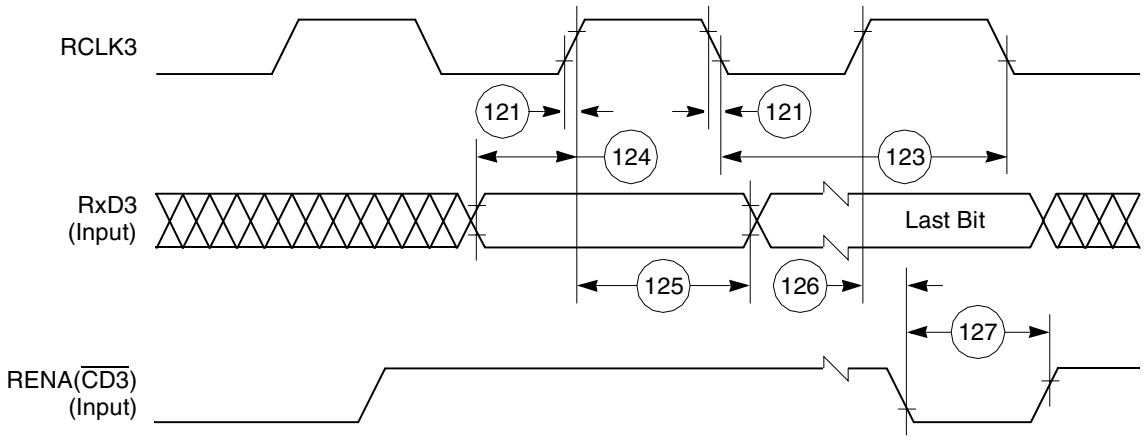
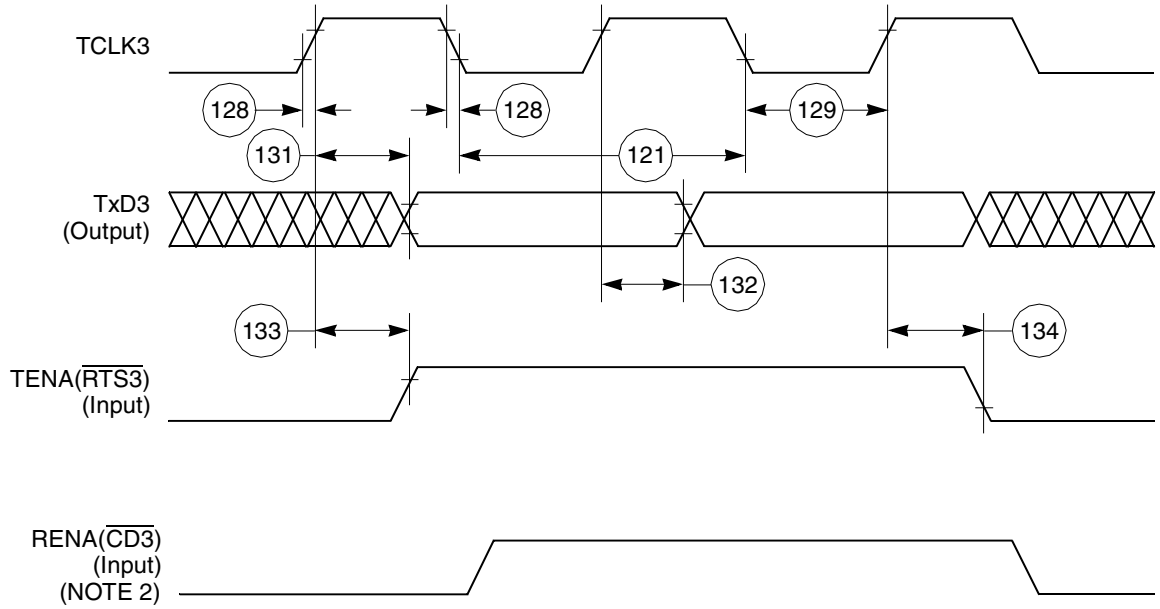


Figure 55. Ethernet Receive Timing Diagram



NOTES:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 56. Ethernet Transmit Timing Diagram

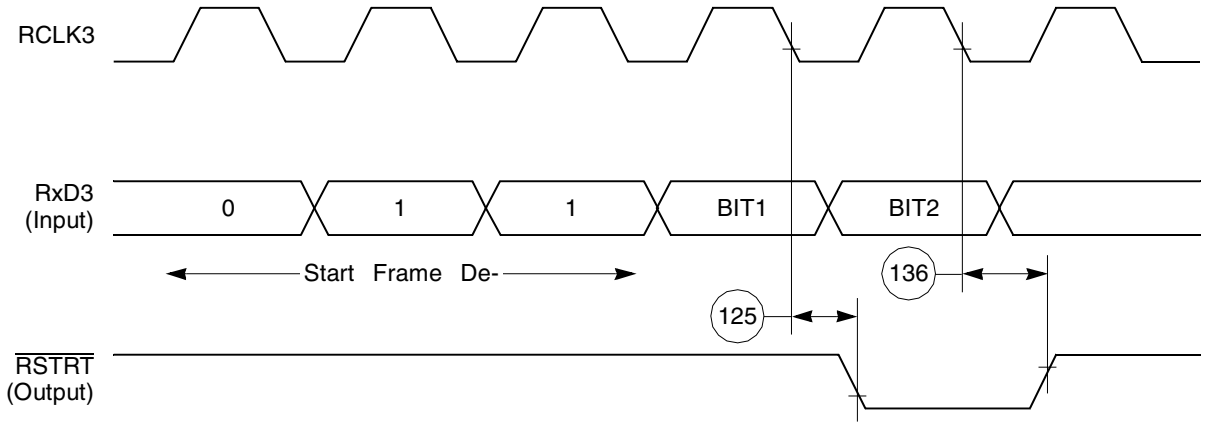


Figure 57. CAM Interface Receive Start Timing Diagram

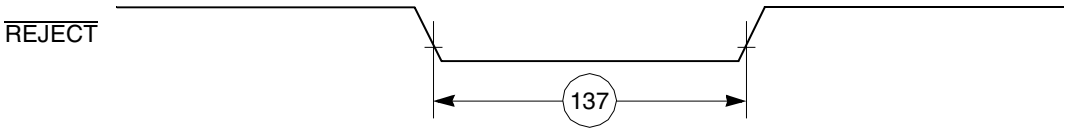


Figure 58. CAM Interface REJECT Timing Diagram

13.8 SPI Master AC Electrical Specifications

Table 24 provides the SPI master timings as shown in Figure 59 and Figure 60.

Table 24. SPI Master Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
160	MASTER cycle time	4	1024	t_{cyc}
161	MASTER clock (SCK) high or low time	2	512	t_{cyc}
162	MASTER data setup time (inputs)	15	—	ns
163	Master data hold time (inputs)	0	—	ns
164	Master data valid (after SCK edge)	—	10	ns
165	Master data hold time (outputs)	0	—	ns
166	Rise time output	—	15	ns
167	Fall time output	—	15	ns

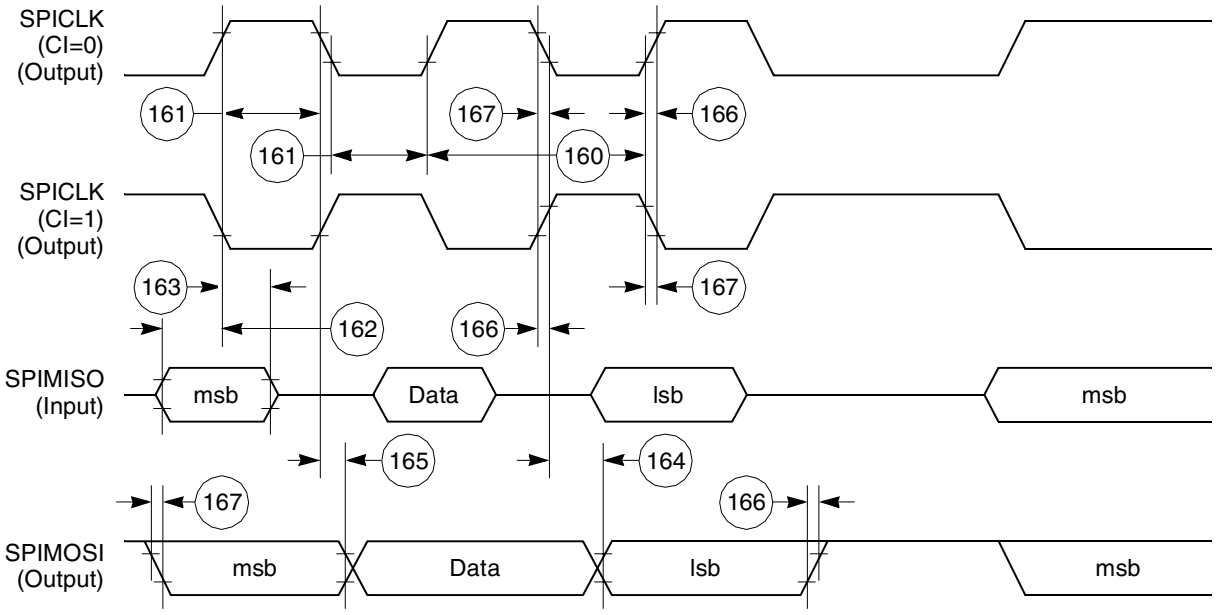


Figure 59. SPI Master (CP = 0) Timing Diagram

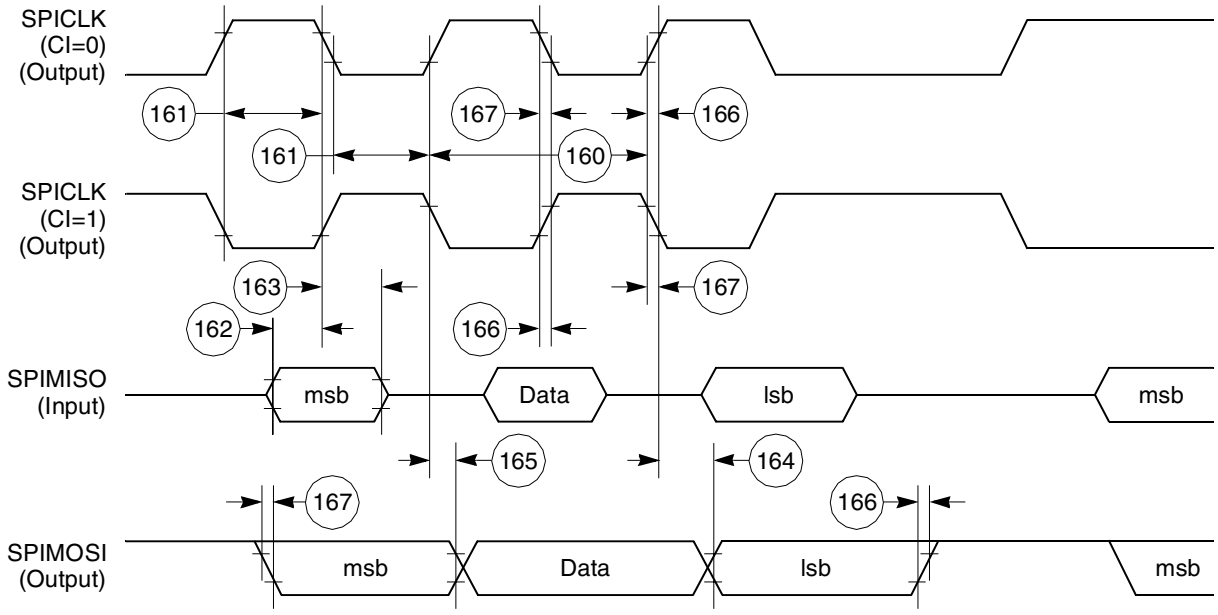


Figure 60. SPI Master (CP = 1) Timing Diagram

13.9 SPI Slave AC Electrical Specifications

Table 25 provides the SPI slave timings as shown in Figure 61 and Figure 62.

Table 25. SPI Slave Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
170	Slave cycle time	2	—	t_{cyc}
171	Slave enable lead time	15	—	ns
172	Slave enable lag time	15	—	ns
173	Slave clock (SPICLK) high or low time	1	—	t_{cyc}
174	Slave sequential transfer delay (does not require deselect)	1	—	t_{cyc}
175	Slave data setup time (inputs)	20	—	ns
176	Slave data hold time (inputs)	20	—	ns
177	Slave access time	—	50	ns

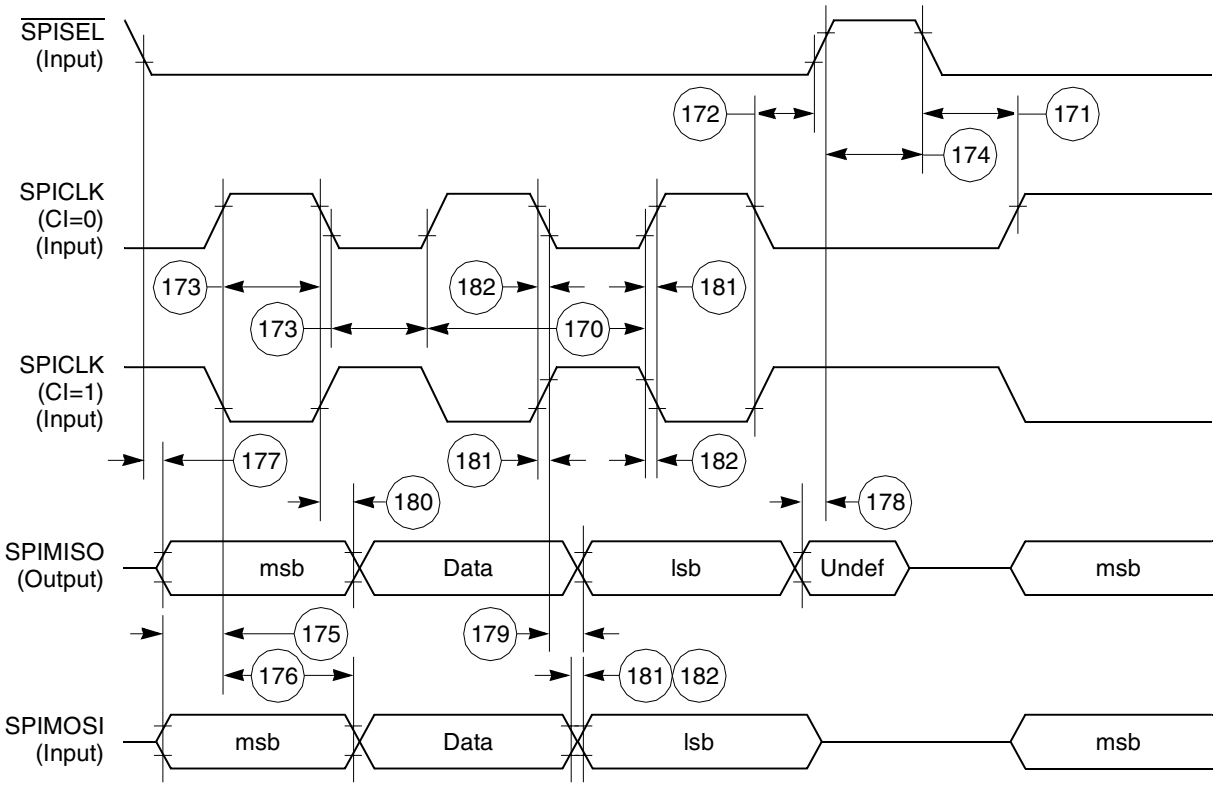


Figure 61. SPI Slave (CP = 0) Timing Diagram

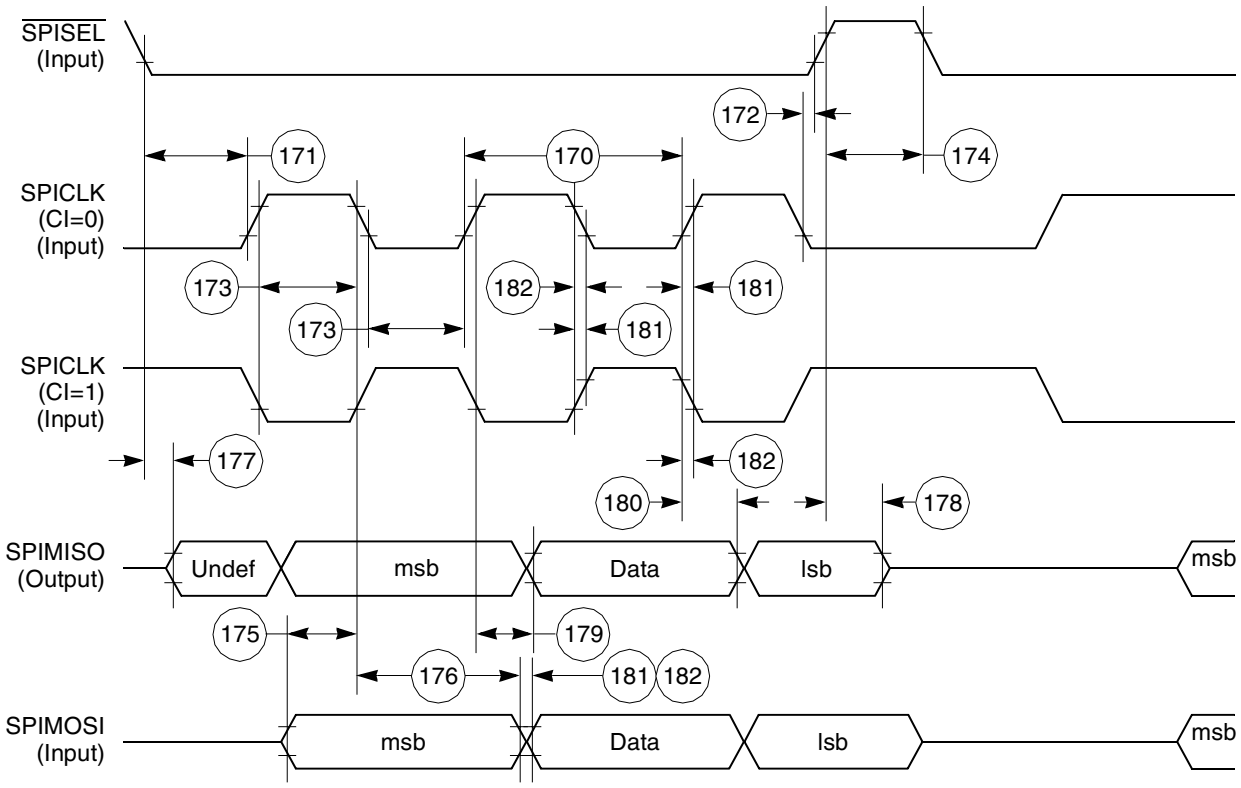


Figure 62. SPI Slave (CP = 1) Timing Diagram

14 FEC Electrical Characteristics

This section provides the AC electrical specifications for the Fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

14.1 MII Receive Signal Timing (MII_RXD[3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%.

Table 26 provides information on the MII receive signal timing.

Table 26. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup	5	—	ns
M2	MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold	5	—	ns
M3	MII_RX_CLK pulse width high	35%	65%	MII_RX_CLK period
M4	MII_RX_CLK pulse width low	35%	65%	MII_RX_CLK period

Figure 63 shows MII receive signal timing.

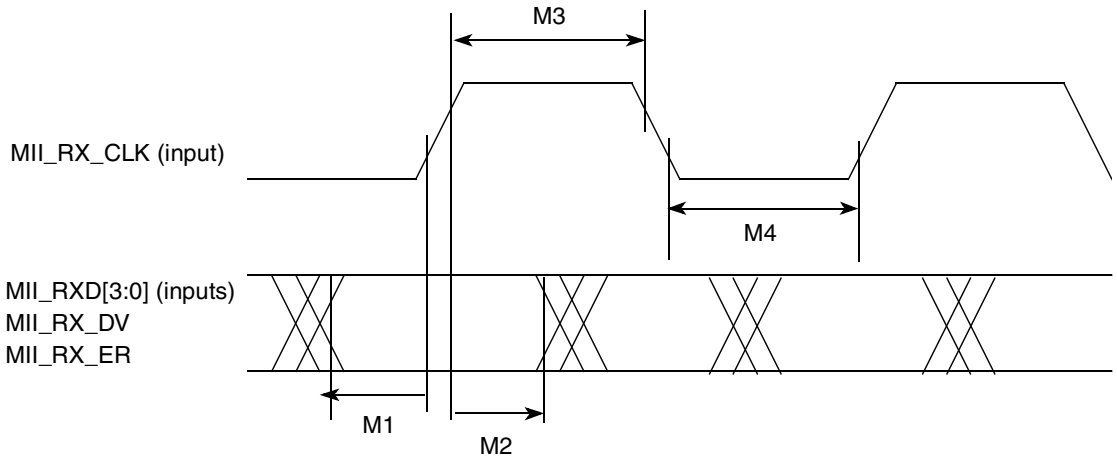


Figure 63. MII Receive Signal Timing Diagram

14.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency – 1%.

Table 27 provides information on the MII transmit signal timing.

Table 27. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid	5	—	ns
M6	MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid	—	25	
M7	MII_TX_CLK pulse width high	35%	65%	MII_TX_CLK period
M8	MII_TX_CLK pulse width low	35%	65%	MII_TX_CLK period

Figure 64 shows the MII transmit signal timing diagram.

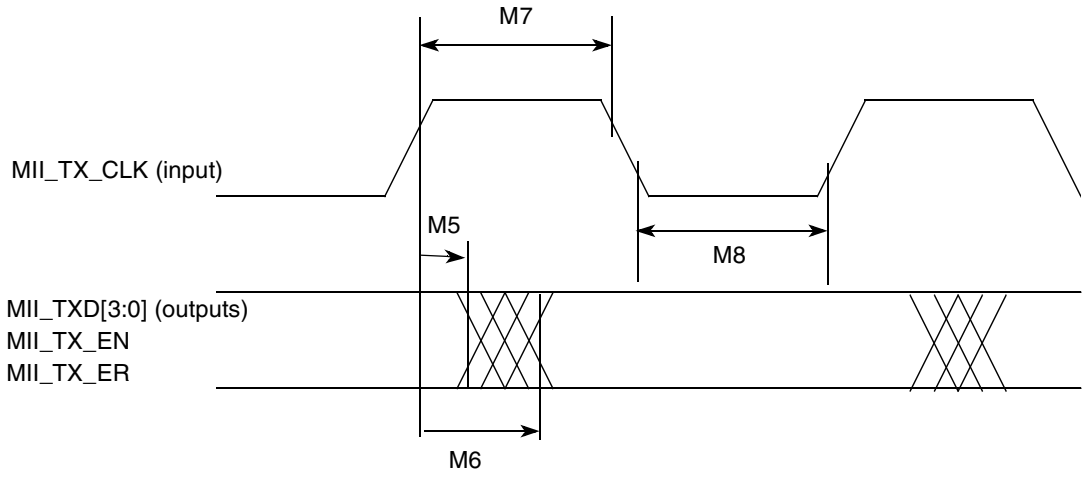


Figure 64. MII Transmit Signal Timing Diagram

14.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 28 provides information on the MII async inputs signal timing.

Table 28. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	MII_CRS, MII_COL minimum pulse width	1.5	—	MII_TX_CLK period

Figure 65 shows the MII asynchronous inputs signal timing diagram.

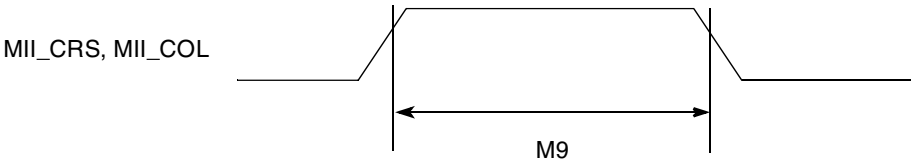


Figure 65. MII Async Inputs Timing Diagram

14.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 29 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

Table 29. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	MII_MDC falling edge to MII_MDIO output valid (max prop delay)	—	25	ns
M12	MII_MDIO (input) to MII_MDC rising edge setup	10	—	ns

Table 29. MII Serial Management Channel Timing (continued)

Num	Characteristic	Min	Max	Unit
M13	MII_MDIO (input) to MII_MDC rising edge hold	0	—	ns
M14	MII_MDC pulse width high	40%	60%	MII_MDC period
M15	MII_MDC pulse width low	40%	60%	MII_MDC period

Figure 66 shows the MII serial management channel timing diagram.

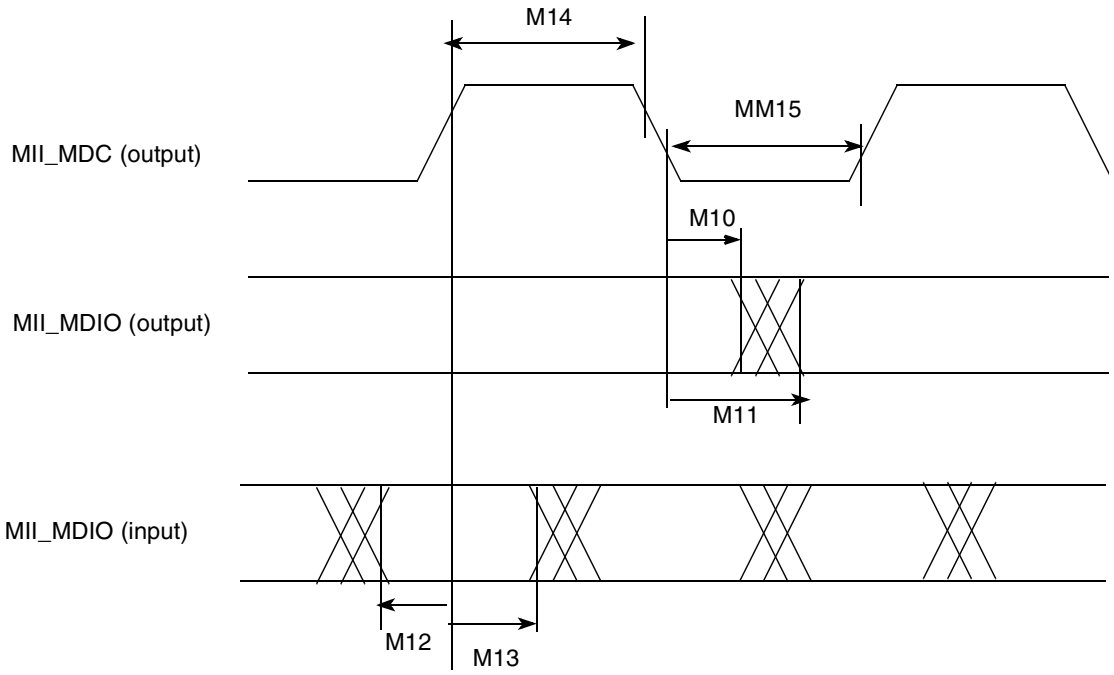


Figure 66. MII Serial Management Channel Timing Diagram

15 Mechanical Data and Ordering Information

Table 30 identifies the packages and operating frequencies orderable for the MPC853T.

Table 30. MPC853T Package/Frequency Orderable

Package Type	Temperature (Tj)	Frequency (MHz)	Order Number
Plastic ball grid array (VR and ZT suffix)	0°C to 95°C	50	MPC853TVR50 MPC853TZT50
		66	MPC853TVR66 MPC853TZT66
		80	MPC853TVR80 MPC853TZT80
		100	MPC853TVR100 MPC853TZT100
Plastic ball grid array (CVR suffix)	–40°C to 100°C	66	TBD

15.1 Pin Assignments

The following sections give the pinout and pin listing for the JEDEC Compliant and the non-JEDEC versions of the 16 x 16 PBGA package.

15.1.1 The JEDEC Compliant Pinout

Figure 67 shows the JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC Family User's Manual*.

NOTE: This is the top view of the device.

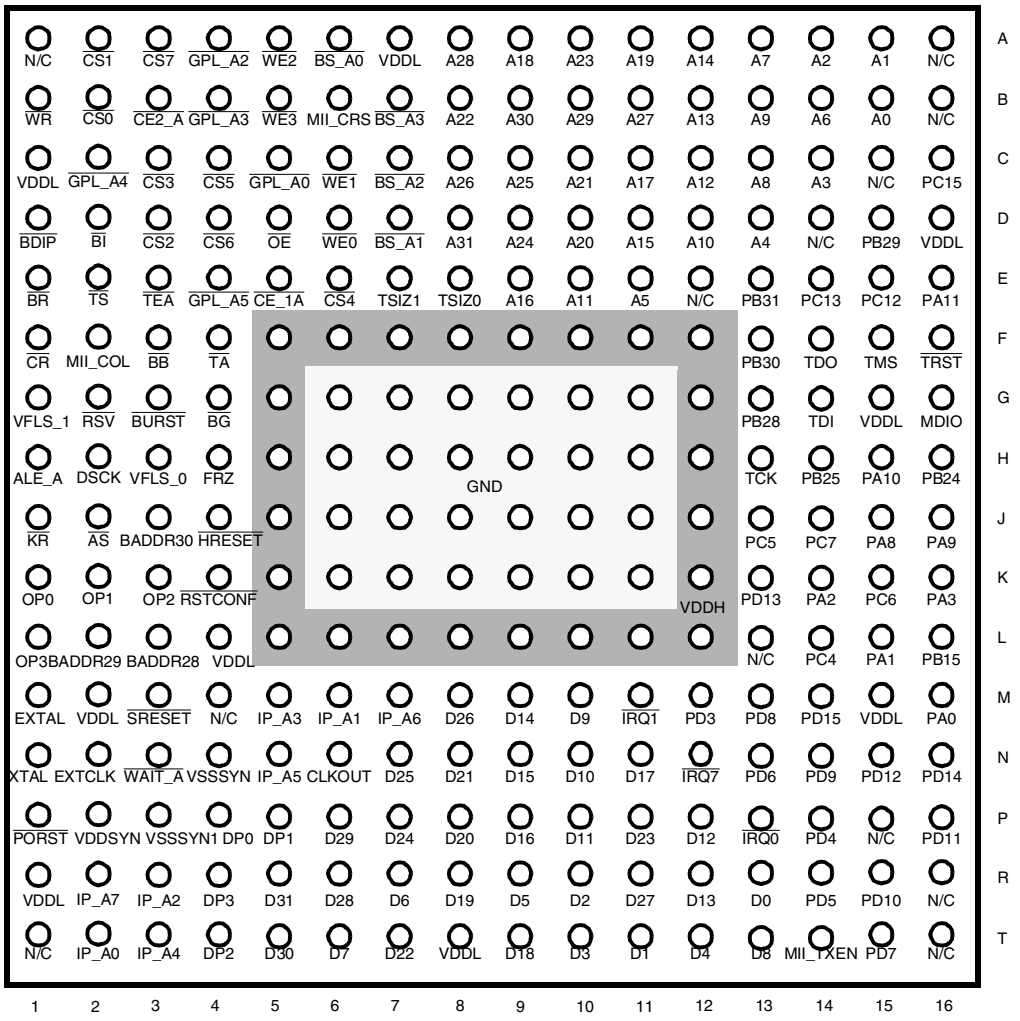


Figure 67. Pinout of the PBGA Package - JEDEC Standard

Table 31 contains a list of the MPC853T input and output signals and shows multiplexing and pin assignments.

Table 31. Pin Assignments - JEDEC Standard

Name	Pin Number	Type
A[0:31]	B15, A15, A14, C14, D13, E11, B14, A13, C13, B13, D12, E10, C12, B12, A12, D11, E9, C11, A9, A11, D10, C10, B8, A10, D9, C9, C8, B11, A8, B10, B9, D8	Bidirectional Three-state (3.3V only)
TSIZ0 $\overline{\text{REG}}$	E8	Bidirectional Three-state (3.3V only)
TSIZ1	E7	Bidirectional Three-state (3.3V only)
RD/$\overline{\text{WR}}$	B1	Bidirectional Three-state (3.3V only)

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
BURST	G3	Bidirectional Three-state (3.3V only)
BDIP GPL_B5	D1	Output
TS	E2	Bidirectional Active Pull-up (3.3V only)
TA	F4	Bidirectional Active Pull-up (3.3V only)
TEA	E3	Open-drain
BI	D2	Bidirectional Active Pull-up (3.3V only)
IRQ2 RSV	G2	Bidirectional Three-state (3.3V only)
IRQ4 KR RETRY SPKROUT	J1	Bidirectional Three-state (3.3V only)
CR IRQ3	F1	Input (3.3V only)
D[0:31]	R13, T11, R10, T10, T12, R9, R7, T6, T13, M10, N10, P10, P12, R12, M9, N9, P9, N11, T9, R8, P8, N8, T7, P11, P7, N7, M8, R11, R6, P6, T5, R5	Bidirectional Three-state (3.3V only)
DP0 IRQ3	P4	Bidirectional Three-state (3.3V only)
DP1 IRQ4	P5	Bidirectional Three-state (3.3V only)
DP2 IRQ5	T4	Bidirectional Three-state (3.3V only)
DP3 IRQ6	R4	Bidirectional Three-state (3.3V only)
BR	E1	Bidirectional (3.3V only)
BG	G4	Bidirectional (3.3V only)
BB	F3	Bidirectional Active Pull-up (3.3V only)
FRZ IRQ6	H4	Bidirectional (3.3V only)
IRQ0	P13	Input (3.3V only)
IRQ1	M11	Input (3.3V only)
M_TX_CLK IRQ7	N12	Input (3.3V only)

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
$\overline{\text{CS}}$[0:5]	B2, A2, D3, C3, E6, C4	Output
$\overline{\text{CS6}}$	D4	Output
$\overline{\text{CS7}}$	A3	Output
$\overline{\text{WE0}}$ BS_B0 $\overline{\text{IORD}}$	D6	Output
$\overline{\text{WE1}}$ BS_B1 $\overline{\text{IOWR}}$	C6	Output
$\overline{\text{WE2}}$ BS_B2 $\overline{\text{PCOE}}$	A5	Output
$\overline{\text{WE3}}$ BS_B3 $\overline{\text{PCWE}}$	B5	Output
$\overline{\text{BS\_A}}$[0:3]	A6, D7, C7, B7	Output
$\overline{\text{GPL\_A0}}$ $\overline{\text{GPL\_B0}}$	C5	Output
$\overline{\text{OE}}$ $\overline{\text{GPL\_A1}}$ $\overline{\text{GPL\_B1}}$	D5	Output
$\overline{\text{GPL\_A}}$[2:3] $\overline{\text{GPL\_B}}$[2:3] $\overline{\text{CS}}$[2–3]	A4, B4	Output
UPWAITA $\overline{\text{GPL\_A4}}$	C2	Bidirectional (3.3V only)
$\overline{\text{GPL\_A5}}$	E4	Output
$\overline{\text{PORESET}}$	P1	Input (3.3V only)
$\overline{\text{RSTCONF}}$	K4	Input (3.3V only)
$\overline{\text{HRESET}}$	J4	Open-drain
$\overline{\text{SRESET}}$	M3	Open-drain
XTAL	N1	Analog Output
EXTAL	M1	Analog Input (1.8V only)
CLKOUT	N6	Output
EXTCLK	N2	Input (1.8V only)
ALE_A	H1	Output
$\overline{\text{CE1\_A}}$	E5	Output
$\overline{\text{CE2\_A}}$	B3	Output

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
WAIT_A	N3	Input (3.3V only)
IP_A0	T2	Input (3.3V only)
IP_A1	M6	Input (3.3V only)
IP_A2 IOIS16_A	R3	Input (3.3V only)
IP_A3	M5	Input (3.3V only)
IP_A4	T3	Input (3.3V only)
IP_A5	N5	Input (3.3V only)
IP_A6	M7	Input (3.3V only)
IP_A7	R2	Input (3.3V only)
DSCK	H2	Bidirectional Three-state (3.3V only)
IWP[0:1] VFLS[0:1]	H3, G1	Bidirectional (3.3V only)
OP0	K1	Bidirectional (3.3V only)
OP1	K2	Output
OP2 MODCK1 STS	K3	Bidirectional (3.3V only)
OP3 MODCK2 DSDO	L1	Bidirectional (3.3V only)
BADDR[28:29]	L3, L2	Output
BADDR30 REG	J3	Output
AS	J2	Input (3.3V only)
PA11 RXD3 L1TXDB	E16	Bidirectional (Optional: Open-drain) (5V tolerant)
PA10 TXD3 L1RXDB	H15	Bidirectional (5V tolerant)
PA9 RXD4	J16	Bidirectional (Optional: Open-drain) (5V tolerant)
PA8 TXD4	J15	Bidirectional (5V tolerant)

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
PA3 CLK5 BRGO3 TIN3	K16	Bidirectional (5V tolerant)
PA2 CLK6 $\overline{\text{TOUT3}}$ L1RCLKB	K14	Bidirectional (5V tolerant)
PA1 CLK7 BRGO4 TIN4	L15	Bidirectional (5V tolerant)
PA0 CLK8 $\overline{\text{TOUT4}}$ L1TCLKB	M16	Bidirectional (5V tolerant)
PB31 $\overline{\text{SPISEL}}$	E13	Bidirectional (Optional: Open-drain) (5V tolerant)
PB30 SPICLK	F13	Bidirectional (Optional: Open-drain) (5V tolerant)
PB29 SPIMOSI	D15	Bidirectional (Optional: Open-drain) (5V tolerant)
PB28 SPIMISO BRGO4	G13	Bidirectional (Optional: Open-drain) (5V tolerant)
PB25 SMTXD1	H14	Bidirectional (Optional: Open-drain) (5V tolerant)
PB24 SMRXD1	H16	Bidirectional (Optional: Open-drain) (5V tolerant)
PB15 BRGO3	L16	Bidirectional (5V tolerant)
PC15 $\overline{\text{DREQ0}}$	C16	Bidirectional (5V tolerant)
PC13 $\overline{\text{RTS3}}$ $\overline{\text{L1RQB}}$ L1ST3	E14	Bidirectional (5V tolerant)

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
PC12 $\overline{\text{RTS4}}$ L1ST4	E15	Bidirectional (5V tolerant)
PC7 L1TSYNCB $\overline{\text{CTS3}}$	J14	Bidirectional (5V tolerant)
PC6 L1RSYNCB $\overline{\text{CD3}}$	K15	Bidirectional (5V tolerant)
PC5 $\overline{\text{CTS4}}$ SDACK1	J13	Bidirectional (5V tolerant)
PC4 $\overline{\text{CD4}}$	L14	Bidirectional (5V tolerant)
PD15 MII-RXD3	M14	Bidirectional (5V tolerant)
PD14 MII-RXD2	N16	Bidirectional (5V tolerant)
PD13 MII-RXD1	K13	Bidirectional (5V tolerant)
PD12 MII-MDC	N15	Bidirectional (5V tolerant)
PD11 RXD3 MII-TXERR	P16	Bidirectional (5V tolerant)
PD10 TXD3 MII-RXD0	R15	Bidirectional (5V tolerant)
PD9 RXD4 MII-TXD0	N14	Bidirectional (5V tolerant)
PD8 TXD4 MII_RX_CLK	M13	Bidirectional (5V tolerant)
PD7 $\overline{\text{RTS3}}$ MII_RX_ER	T15	Bidirectional (5V tolerant)
PD6 $\overline{\text{RTS4}}$ MII_RX_DV	N13	Bidirectional (5V tolerant)

Table 31. Pin Assignments - JEDEC Standard (continued)

Name	Pin Number	Type
PD5 MII-TXD3	R14	Bidirectional (5V tolerant)
PD4 MII-TXD2	P14	Bidirectional (5V tolerant)
PD3 MII-TXD1	M12	Bidirectional (5V tolerant)
TMS	F15	Input (5V tolerant)
TDI DSDI	G14	Input (5V tolerant)
TCK DSCK	H13	Input (5V tolerant)
$\overline{\text{TRST}}$	F16	Input (5V tolerant)
TDO DSDO	F14	Output (5V tolerant)
MII_CRS	B6	Input
MII_MDIO	G16	Bidirectional (5V tolerant)
MII_TXEN	T14	Output (5V tolerant)
MII_COL	F2	Input
V_{SSSYN}	N4	PLL analog GND
V_{SSSYN1}	P3	PLL analog GND
V_{DDSYN}	P2	PLL analog V_{DD}
GND	G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11	Power
VDDL	A7, C1, D16, G15, L4, M2, R1, M15, T8	Power
VDDH	F5, F6, F7, F8, F9, F10, F11, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L6, L7, L8, L9, L10, L11, L12	Power
N/C	A1, A16, B16, C15, D14, E12, L13, M4, P15, R16, T1, T16	No-connect

15.1.2 The Non-JEDEC Pinout

Figure 68 shows the non-JEDEC pinout of the PBGA package as viewed from the top surface. For additional information, see the *MPC866 PowerQUICC Family User's Manual*.

NOTE: This is the top view of the device.

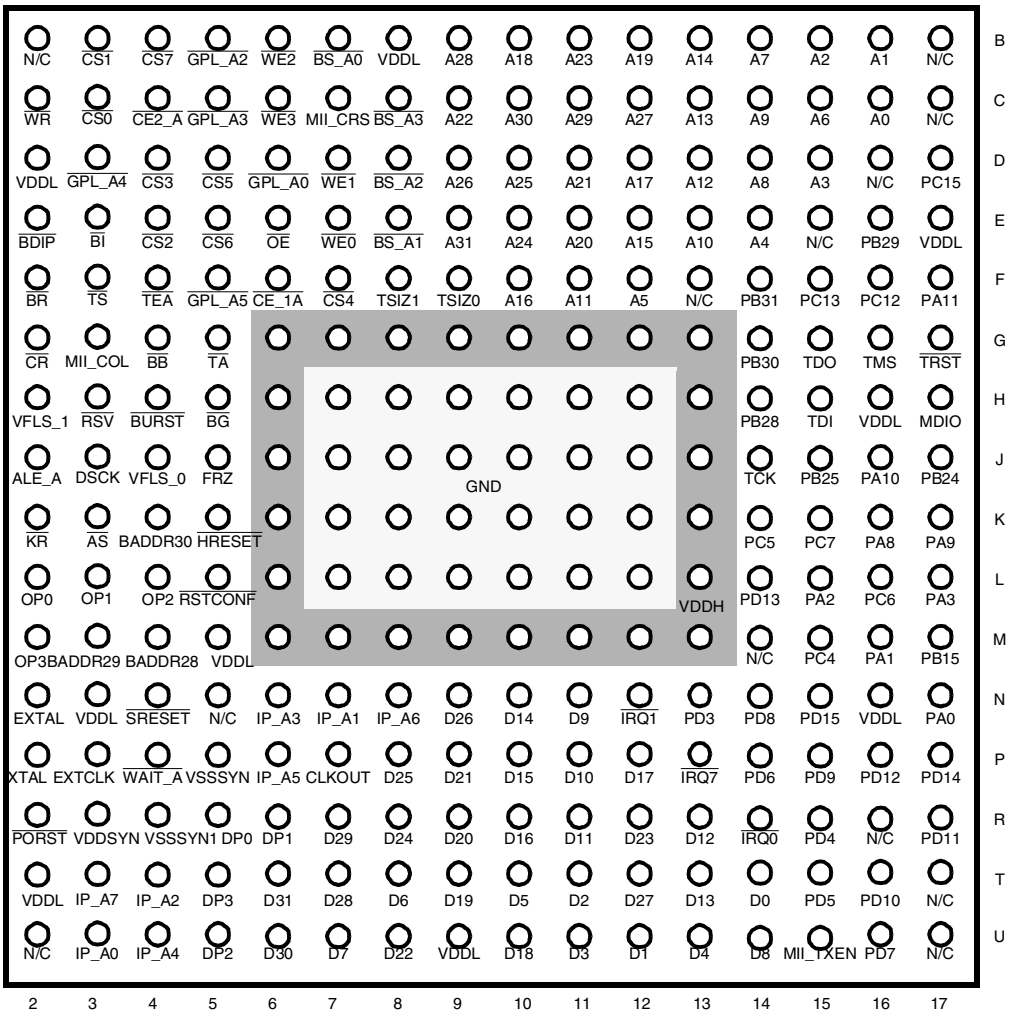


Figure 68. Pinout of the PBGA Package—non-JEDEC

Table 32 contains a list of the MPC853T input and output signals and shows multiplexing and pin assignments.

Table 32. Pin Assignments—Non-JEDEC

Name	Pin Number	Type
A[0:31]	C16, B16, B15, D15, E14, F12, C15, B14, D14, C14, E13, F11, D13, C13, B13, E12, F10, D12, B10, B12, E11, D11, C9, B11, E10, D10, D9, C12, B9, C11, C10, E9	Bidirectional Three-state (3.3 V only)
TSIZ0 REG	F9	Bidirectional Three-state (3.3 V only)
TSIZ1	F8	Bidirectional Three-state (3.3 V only)
RD/WR	C2	Bidirectional Three-state (3.3 V only)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
$\overline{\text{BURST}}$	H4	Bidirectional Three-state (3.3 V only)
$\overline{\text{BDIP}}$ $\overline{\text{GPL\_B5}}$	E2	Output
$\overline{\text{TS}}$	F3	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{TA}}$	G5	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{TEA}}$	F4	Open drain
$\overline{\text{BI}}$	E3	Bidirectional Active pull-up (3.3 V only)
$\overline{\text{IRQ2}}$ $\overline{\text{RSV}}$	H3	Bidirectional Three-state (3.3 V only)
$\overline{\text{IRQ4}}$ $\overline{\text{KR}}$ $\overline{\text{RETRY}}$ SPKROUT	K2	Bidirectional Three-state (3.3 V only)
$\overline{\text{CR}}$ $\overline{\text{IRQ3}}$	G2	Input (3.3 V only)
D[0:31]	T14, U12, T11, U11, U13, T10, T8, U7, U14, N11, P11, R11, R13, T13, N10, P10, R10, P12, U10, T9, R9, P9, U8, R12, R8, P8, N9, T12, T7, R7, U6, T6	Bidirectional Three-state (3.3 V only)
DP0 $\overline{\text{IRQ3}}$	R5	Bidirectional Three-state (3.3 V only)
DP1 $\overline{\text{IRQ4}}$	R6	Bidirectional Three-state (3.3 V only)
DP2 $\overline{\text{IRQ5}}$	U5	Bidirectional Three-state (3.3 V only)
DP3 $\overline{\text{IRQ6}}$	T5	Bidirectional Three-state (3.3 V only)
$\overline{\text{BR}}$	F2	Bidirectional (3.3 V only)
$\overline{\text{BG}}$	H5	Bidirectional (3.3 V only)
$\overline{\text{BB}}$	G4	Bidirectional Active pull-up (3.3 V only)
FRZ $\overline{\text{IRQ6}}$	J5	Bidirectional (3.3 V only)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
IRQ0	R14	Input (3.3 V only)
IRQ1	N12	Input (3.3 V only)
IRQ7 M_TX_CLK	P13	Input (3.3 V only)
CS[0:5]	C3, B3, E4, D4, F7, D5	Output
CS6	E5	Output
CS7	B4	Output
WE0 BS_B0 IORD	E7	Output
WE1 BS_B1 IOWR	D7	Output
WE2 BS_B2 PCOE	B6	Output
WE3 BS_B3 PCWE	C6	Output
BS_A[0:3]	B7, E8, D8, C8	Output
GPL_A0 GPL_B0	D6	Output
OE GPL_A1 GPL_B1	E6	Output
GPL_A[2:3] GPL_B[2:3] CS[2–3]	B5, C5	Output
UPWAITA GPL_A4	D3	Bidirectional (3.3 V only)
GPL_A5	F5	Output
PORESET	R2	Input (3.3 V only)
RSTCONF	L5	Input (3.3 V only)
HRESET	K5	Open drain
SRESET	N4	Open drain
XTAL	P2	Analog output
EXTAL	N2	Analog Input (3.3 V only)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
CLKOUT	P7	Output
EXTCLK	P3	Input (3.3 V only)
ALE_A	J2	Output
$\overline{\text{CE1\_A}}$	F6	Output
$\overline{\text{CE2\_A}}$	C4	Output
$\overline{\text{WAIT\_A}}$	P4	Input (3.3 V only)
IP_A0	U3	Input (3.3 V only)
IP_A1	N7	Input (3.3 V only)
IP_A2 $\overline{\text{IOIS16\_A}}$	T4	Input (3.3 V only)
IP_A3	N6	Input (3.3 V only)
IP_A4	U4	Input (3.3 V only)
IP_A5	P6	Input (3.3 V only)
IP_A6	N8	Input (3.3 V only)
IP_A7	T3	Input (3.3 V only)
DSCK	J3	Bidirectional Three-state (3.3 V only)
IWP[0:1] VFLS[0:1]	J4, H2	Bidirectional (3.3 V only)
OP0	L2	Bidirectional (3.3 V only)
OP1	L3	Output
OP2 MODCK1 $\overline{\text{STS}}$	L4	Bidirectional (3.3 V only)
OP3 MODCK2 DSDO	M2	Bidirectional (3.3 V only)
BADDR[28:29]	M4, M3	Output
BADDR30 $\overline{\text{REG}}$	K4	Output
$\overline{\text{AS}}$	K3	Input (3.3 V only)
PA11 RXD3 L1TXDB	F17	Bidirectional (Optional: open-drain) (5-V tolerant)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
PA10 TXD3 L1RXDB	J16	Bidirectional (Optional: open-drain) (5-V tolerant)
PA9 RXD4	K17	Bidirectional (Optional: open-drain) (5-V tolerant)
PA8 TXD4	K16	Bidirectional (Optional: open-drain) (5-V tolerant)
PA3 CLK5 BRGO3 TIN3	L17	Bidirectional (5-V tolerant)
PA2 CLK6 $\overline{\text{TOUT3}}$ L1RCLKB	L15	Bidirectional (5-V tolerant)
PA1 CLK7 BRGO4 TIN4	M16	Bidirectional (5-V tolerant)
PA0 CLK8 $\overline{\text{TOUT4}}$ L1TCLKB	N17	Bidirectional (5-V tolerant)
PB31 $\overline{\text{SPISEL}}$	F14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB30 SPICLK	G14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB29 SPIMOSI	E16	Bidirectional (Optional: open-drain) (5-V tolerant)
PB28 SPIMISO BRGO4	H14	Bidirectional (Optional: open-drain) (5-V tolerant)
PB25 SMTXD1	J15	Bidirectional (Optional: open-drain) (5-V tolerant)

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
PB24 SMRXD1	J17	Bidirectional (Optional: open-drain) (5-V tolerant)
PB15 BRGO3	M17	Bidirectional (5-V tolerant)
PC15 $\overline{\text{DREQ0}}$	D17	Bidirectional (5-V tolerant)
PC13 $\overline{\text{RTS3}}$ $\overline{\text{L1RQB}}$ L1ST3	F15	Bidirectional (5-V tolerant)
PC12 $\overline{\text{RTS4}}$ L1ST4	F16	Bidirectional (5-V tolerant)
PC7 L1TSYNCB $\overline{\text{CTS3}}$	K15	Bidirectional (5-V tolerant)
PC6 L1RSYNCB $\overline{\text{CD3}}$	L16	Bidirectional (5-V tolerant)
PC5 $\overline{\text{CTS4}}$ SDACK1	K14	Bidirectional (5-V tolerant)
PC4 $\overline{\text{CD4}}$	M15	Bidirectional (5-V tolerant)
PD15 MII_RXD3	N15	Bidirectional (5-V tolerant)
PD14 MII_RXD2	P17	Bidirectional (5-V tolerant)
PD13 MII_RXD1	L14	Bidirectional (5-V tolerant)
PD12 MII_MDC	P16	Bidirectional (5-V tolerant)
PD11 RXD3 MII_TX_ER	R17	Bidirectional (5-V tolerant)
PD10 TXD3 MII_RXD0	T16	Bidirectional (5-V tolerant)

Table 32. Pin Assignments—Non-JEDEC (continued)

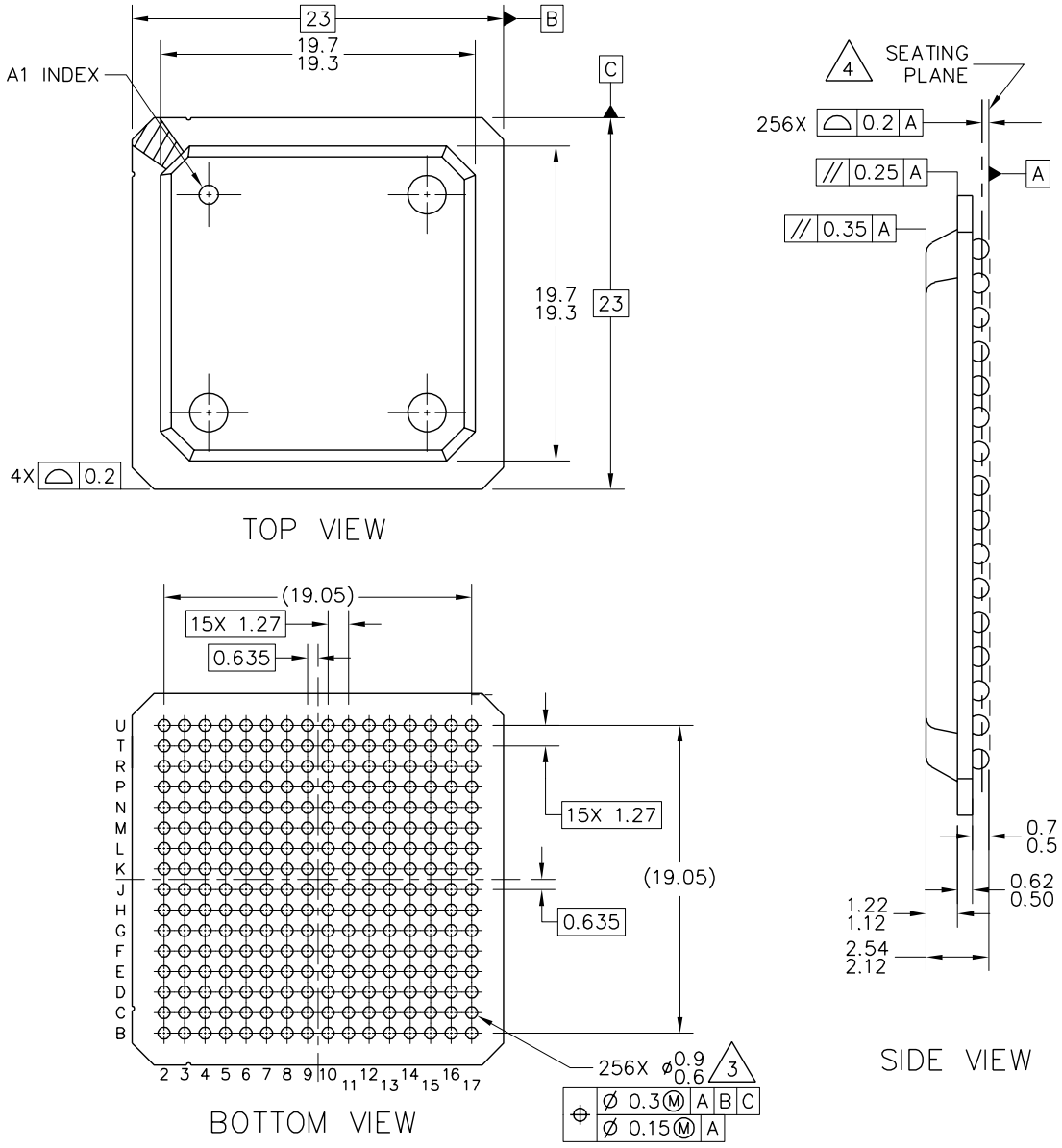
Name	Pin Number	Type
PD9 RXD4 MII_TXD0	P15	Bidirectional (5-V tolerant)
PD8 TXD4 MII_RX_CLK	N14	Bidirectional (5-V tolerant)
PD7 $\overline{\text{RTS3}}$ MII_RX_ER	U16	Bidirectional (5-V tolerant)
PD6 $\overline{\text{RTS4}}$ MII_RX_DV	P14	Bidirectional (5-V tolerant)
PD5 MII_TXD3	T15	Bidirectional (5-V tolerant)
PD4 MII_TXD2	R15	Bidirectional (5-V tolerant)
PD3 MII_TXD1	N13	Bidirectional (5-V tolerant)
TMS	G16	Input (5-V tolerant)
TDI DSDI	H15	Input (5-V tolerant)
TCK DSCK	J14	Input (5-V tolerant)
$\overline{\text{TRST}}$	G17	Input (5-V tolerant)
TDO DSDO	G15	Output (5-V tolerant)
MII_CRS	C7	Input
MII_MDIO	H17	Bidirectional (5-V tolerant)
MII_TX_EN	U15	Output (5-V tolerant)
MII_COL	G3	Input
V_{SSSYN}	P5	PLL analog GND
V_{SSSYN1}	R4	PLL analog GND
V_{DDSYN}	R3	PLL analog V_{DD}

Table 32. Pin Assignments—Non-JEDEC (continued)

Name	Pin Number	Type
GND	H7, H8, H9, H10, H11, H12, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10, K11, K12, L7, L8, L9, L10, L11, L12	Power
V_{DDL}	B8, D2, E17, H16, M5, N3, T2, N16, U9	Power
V_{DDH}	G6, G7, G8, G9, G10, G11, G12, G13, H6, H13, J6, J13, K6, K13, L6, L13, M6, M7, M8, M9, M10, M11, M12, M13	Power
N/C	B2, B17, C17, D16, E15, F13, M14, N5, R16, T17, U2, U17	No-connect

15.2 Mechanical Dimensions of the PBGA Package

Figure 69 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Note: Solder sphere composition is 95.5%Sn 45%Ag 0.5%Cu for MPC853TVRXXX
Solder sphere composition is 62%Sn 36%Pb 2%Ag for MPC853TZTXXX

Figure 69. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

16 References

Semiconductor Equipment and Materials International 805 East Middlefield Rd Mountain View, CA 94043	(415) 964-5111
MIL-SPEC and EIA/JESD (JEDEC) specifications (Available from Global Engineering Documents)	800-854-7179 or 303-397-7956
JEDEC Specifications	http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

17 Document Revision History

Table 33 lists significant changes between revisions of this hardware specification.

Table 33. Document Revision History

Revision Number	Date	Changes
0	10/2003	Initial release.
0.1	12/2003	Added overbars to signals CR (pin G2) and WAIT_A (pin P4) on Figure 62 on page 63.
1.0	12/2004	• Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values • Added a footnote to Spec 41 specifying that EDM = 1 • Broke the Section 15.1, “Pin Assignments” into 2 smaller sections for the JEDEC and non-JEDEC pinouts.

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