CLR-HSMC

User Manual

Terasic CLR-HSMC Daughter Card

CONTENTS

Introduction

CLR-HSMC is designed to provide Camera Link connections which are communication interfaces for vision applications. It uses the High Speed Mezzanine Card (HSMC) to interface with other mother board hosting HSMC/HSTC carrier such as DE4, DE3 and DE2-115.

1.1 Features

Figure 1-1 shows the photo of the CLR-HSMC board. The important features are listed below:

- Support of standard Camera Link modes (base, medium, dual base assembly)

- Serial Communication with camera

- Simple interface

- Automatic detection by hardware / software

- Two LVDS 28-bit channel link chip (DS90CR288A)

  ◦ 28 bit, 20 to 85 MHz shift clock support

  ◦ Up to 2.38 Gbps throughput

  ◦ Up to 297.5 Mbytes/sec bandwidth

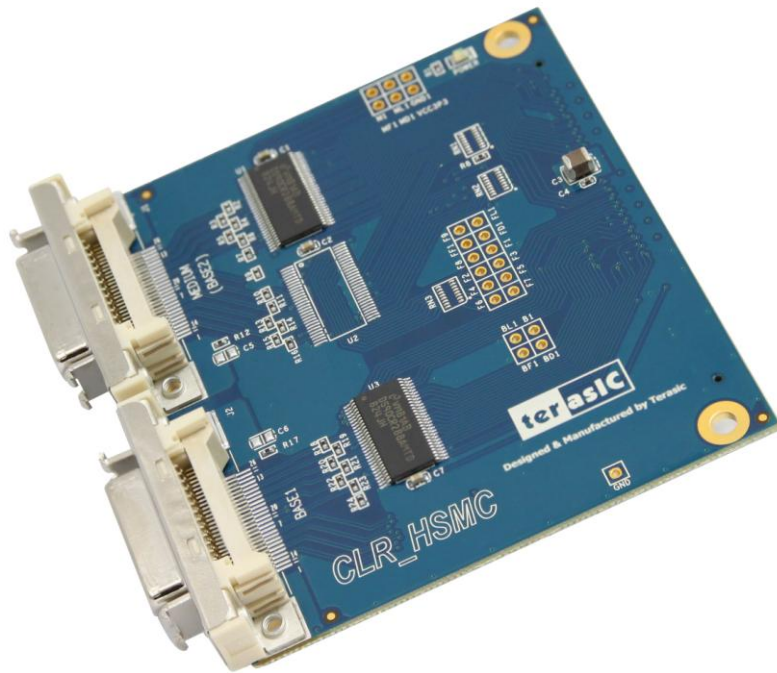- Support 2.5V and 3.3 V I/O standard

Figure 1-1 Picture of the CLR-HSMC Board

1.2 Getting Help

Here are some places to get help if you encounter any problem:

- Email to support@terasic.com

- Taiwan & China: +886-3-550-8800

- Korea : +82-2-512-7661

- Japan: +81-428-77-7000

Chapter 2

Architecture & Configuration

This chapter describes the architecture and configuration of the CLR-HSMC board including block diagram and components.
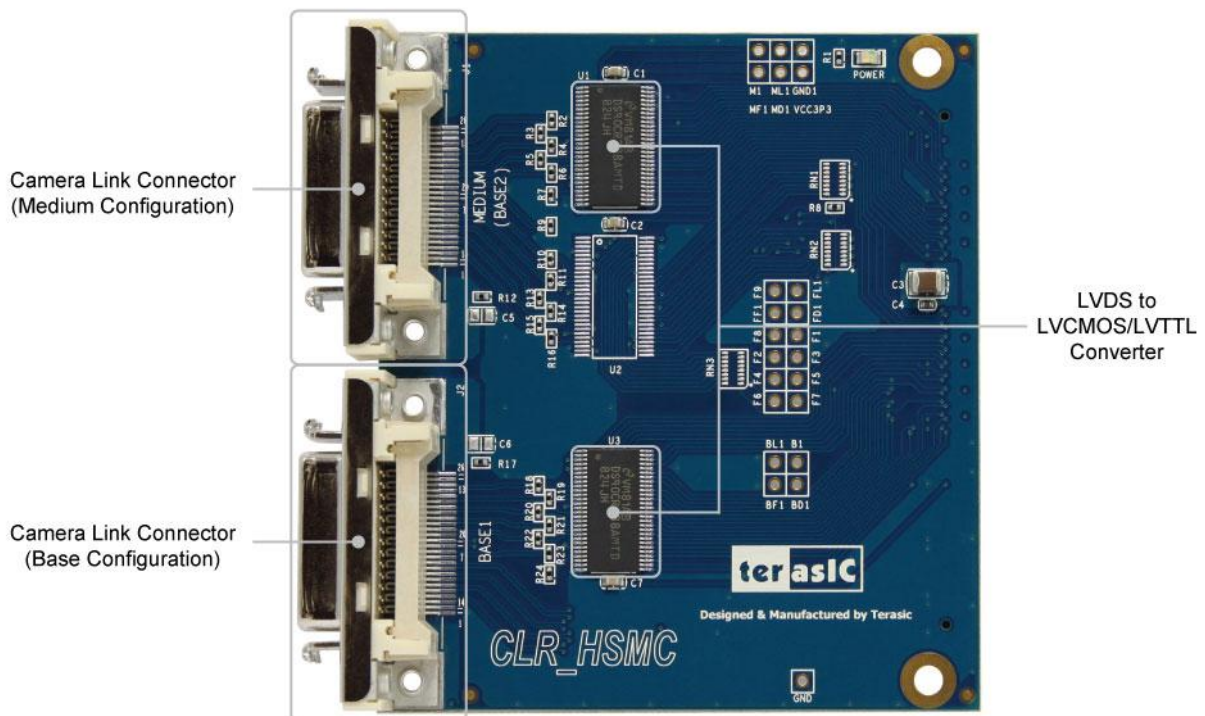

Figure 2-1 The CLR-HSMC Board PCB and Component Diagram

A photograph of the CLR-HSMC is shown in **Figure 2-1** and **Figure 2-2**. It depicts the layout of the board and indicates the location of the connectors and key components.
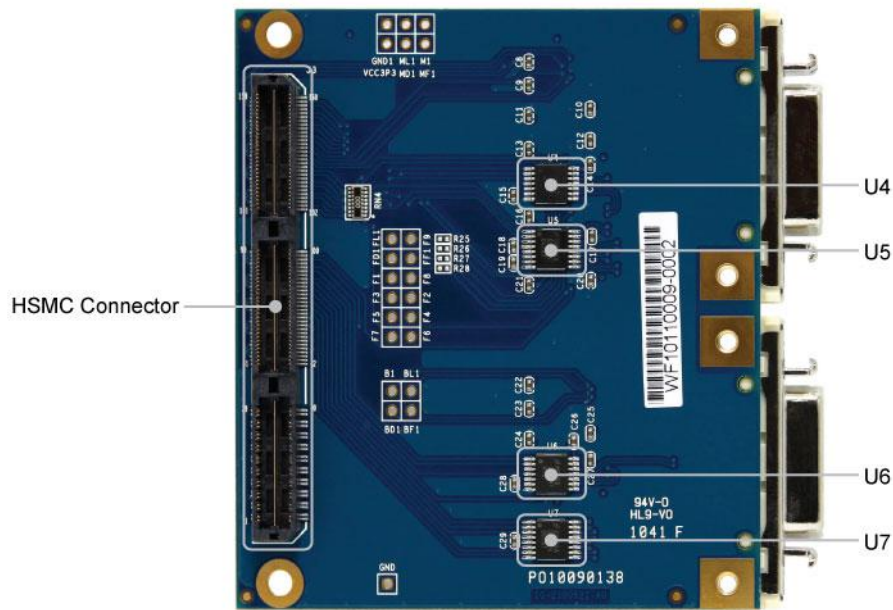
Figure 2-2 The CLR-HSMC Board Back Side

The following components are provided on the CLR-HSMC board:

- National Semiconductor DS90CR288A for LVDS to LVTTL adapting of data signals. (U1, U3,)

- National Semiconductor DS90LV047A for LVDS to LVTTL adapting of control signals. (U5, U7)

- National Semiconductor DS90LV019 for LVDS to LVTTL adapting of serial control signals. (U4, U6)

2.1 Block Diagram

Figure 2-3 shows the block diagram of the CLR-HSMC board in base mode configuration.
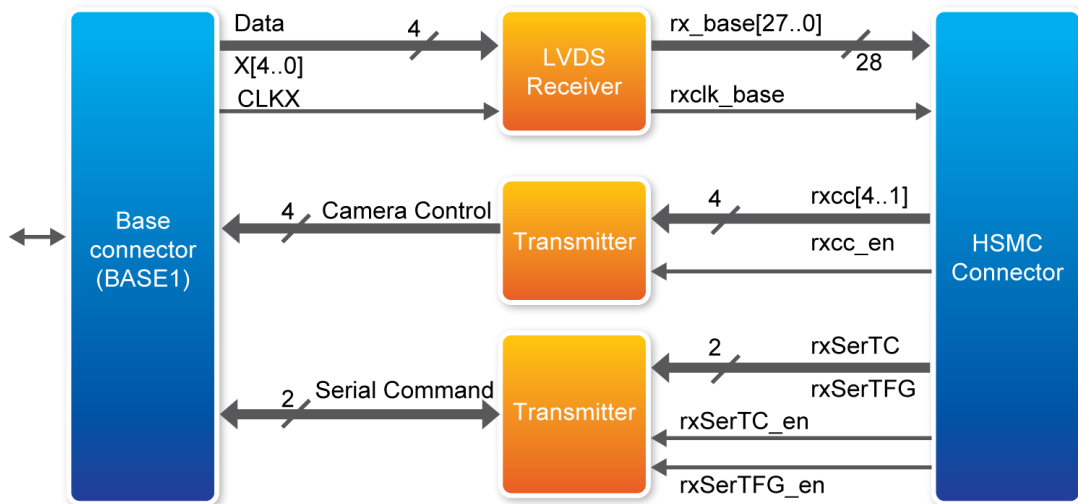
Figure 2-3 Block Diagram of the CLR-HSMC Board (Base Mode)

Figure 2-4 shows the block diagram of the CLR-HSMC board in medium mode configuration.
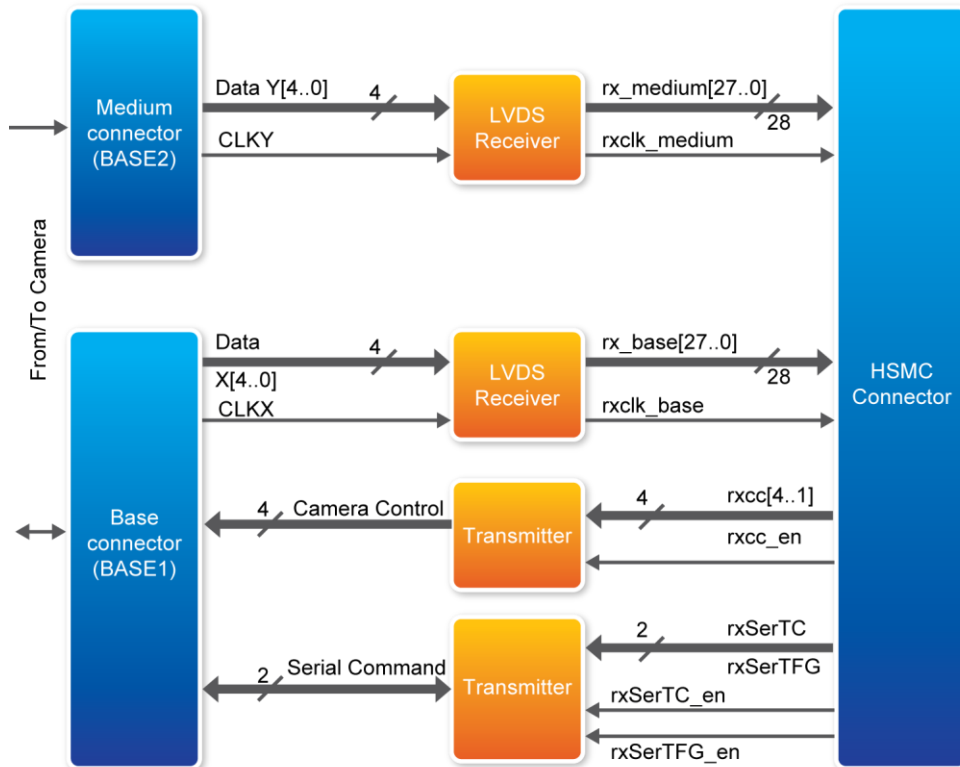
Figure 2-4 Block Diagram of the CLR-HSMC Board (Medium Mode)

Figure 2-5 shows the block diagram of the CLR-HSMC board in dual-base mode configuration.
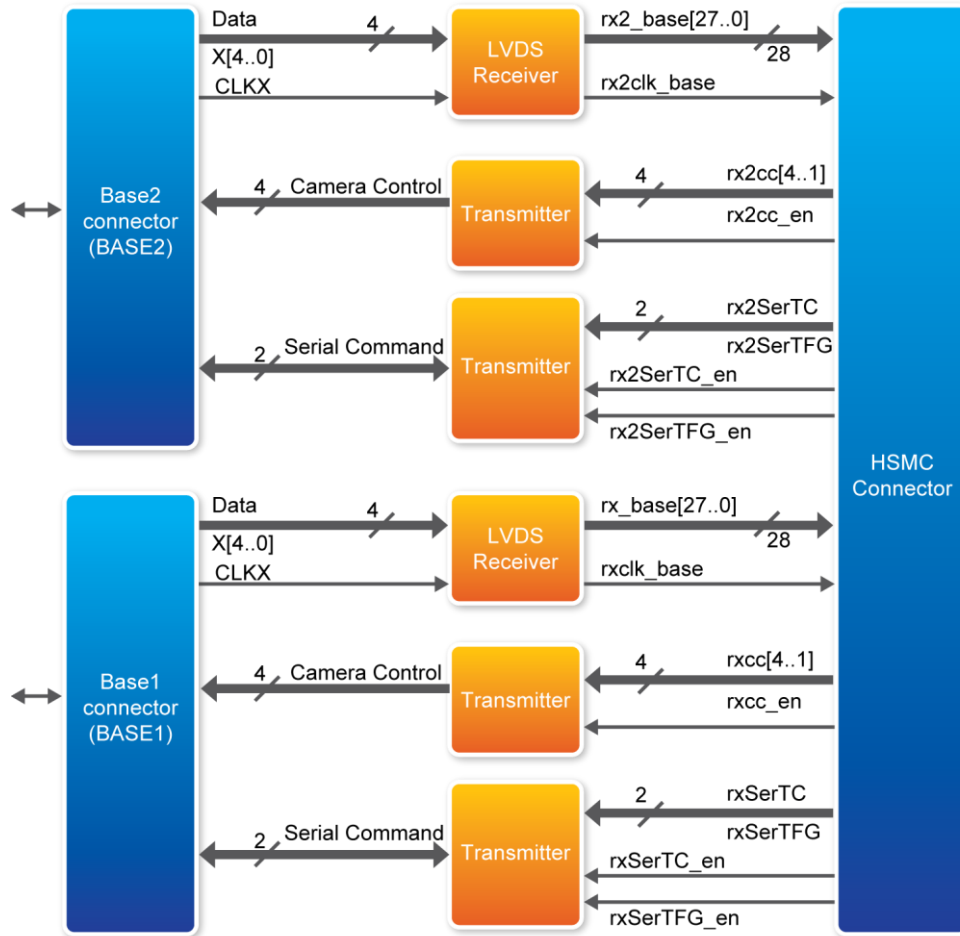
Figure 2-5 Block Diagram of the CLR-HSMC Board (Dual-base Mode)

2.2 Connectivity

The CLR-HSMC offers connectivity to any HSMC-based host boards including the DE4, DE3 and DE2-115.
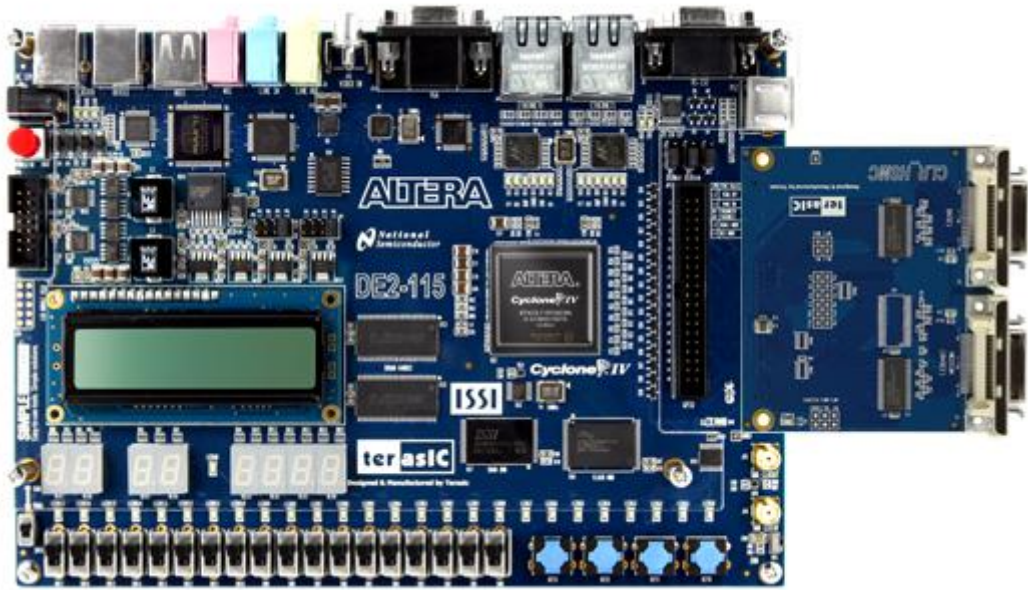
Figure 2-6 Camera Link Receiver Card connection to the Altera DE2-115 Development Board
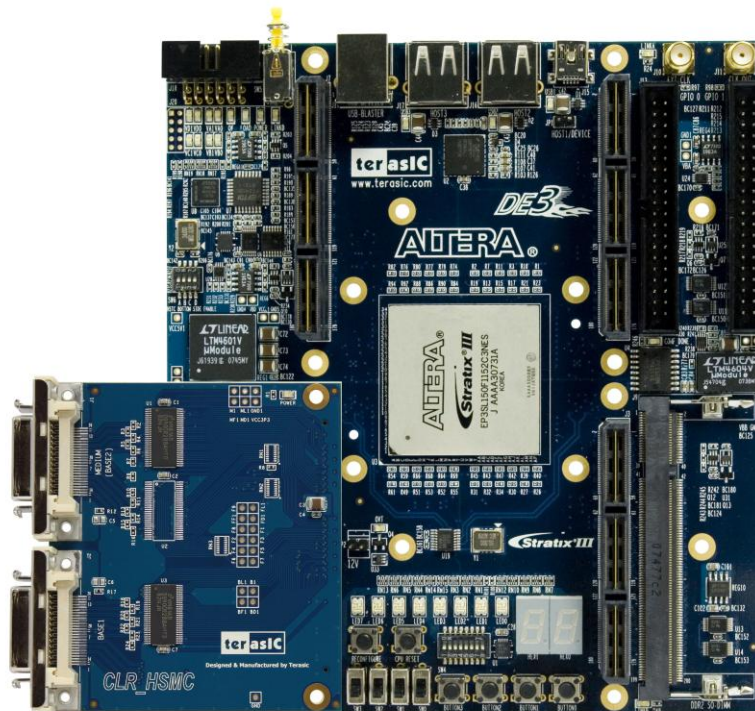
Figure 2-7 Camera Link Receiver Card connection to the Altera DE3 Development System
Note. An adapter (HFF) is required to connect CLR-HSMC with DE3. It is bundled in DE3 kit.

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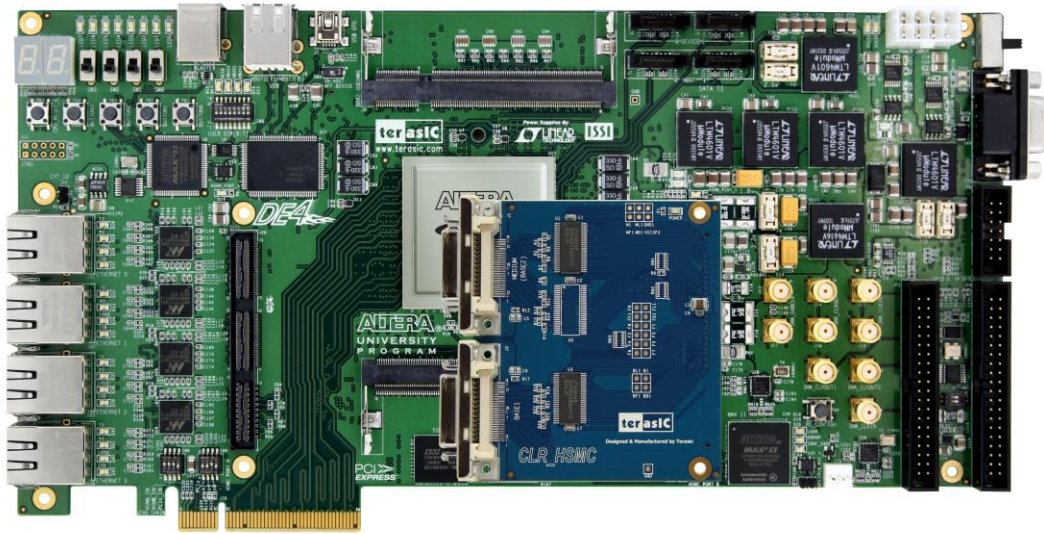
Figure 2-8 **Camera Link Receiver Card connection to Altera DE4 Development and Education Board**

Note. An adapter (HMF2) is required to connect CLR-HSMC with DE4. It is bundled in DE4 kit.

Chapter 3

Pin Description

This chapter describes the detailed information of the connector interfaces, and the pin description on the CLR-HSMC board.

3.1 HSMC Expansion Connector

The CLR-HSMC board contains a HSMC connector. **Figure 3-1**, **Figure 3-2** and **Figure 3-3** show the pin-outs of the HSMC connector on the CLR-HSMC board.

The voltage level of the I/O pin on the HSMC connector can support to 3.3V and 2.5V, because the DS90CR288A VIH are as low as 2.0V (Please refer to the DS90CR288A's datasheets)

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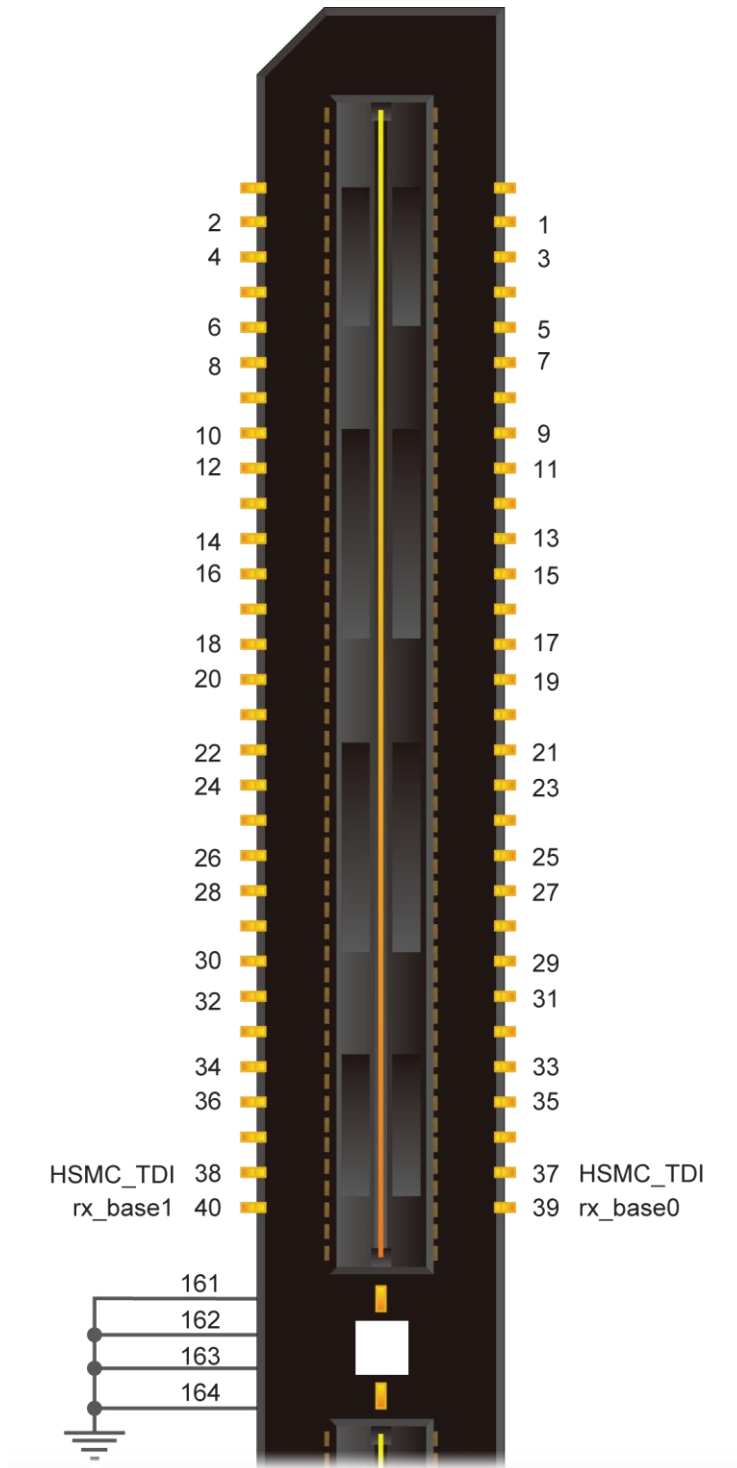
Figure 3-1 Pin-outs of Bank 1 on the HSMC Connector
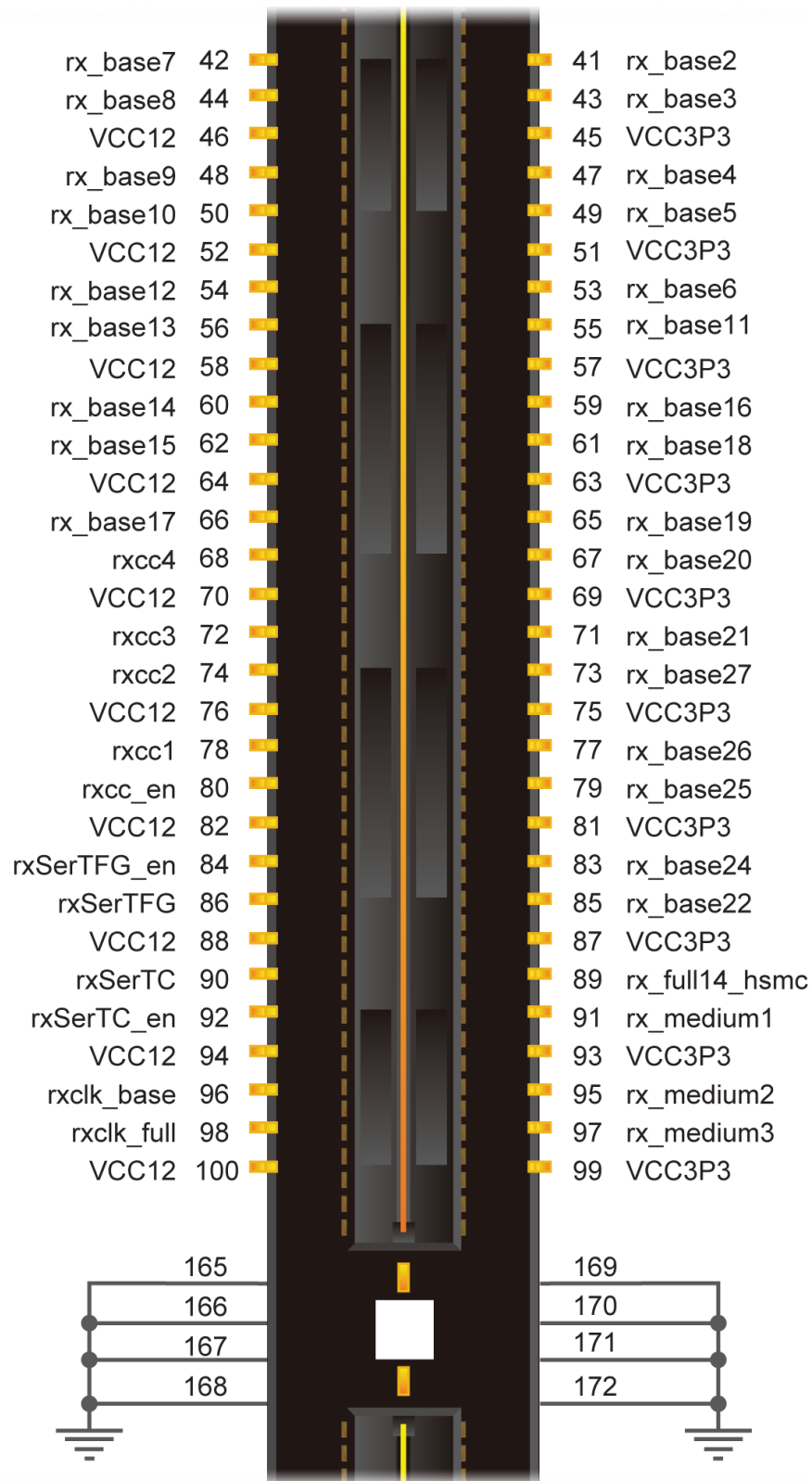
Figure 3-2 Pin-outs of Bank 2 on the HSMC Connector

rx2SerTC_en	102	101	rx_medium4
rxSerTFG	104	103	rx_medium5
VCC12	106	105	VCC3P3
rx2SerTFG_en	108	107	rx_medium6
rx2cc1	110	109	rx_medium7
VCC12	112	111	VCC3P3
rx2cc2	114	113	rx_medium8
rx2cc3	116	115	rx_medium9
VCC12	118	117	VCC3P3
rx2cc4	120	119	rx_medium10
rx2cc_en	122	121	rx_medium11
VCC12	124	123	VCC3P3
rx_medium0	126	125	rx_medium12
rx_medium27	128	127	rx_medium13
VCC12	130	129	VCC3P3
rx_medium26	132	131	rx_medium14
rx_medium25	134	133	rx_medium15
VCC12	136	135	VCC3P3
rx2SerTC_en	138	137	rx_medium16
rx_full9_hsmc	140	139	rx_medium17
VCC12	142	141	VCC3P3
rx_full10_hsmc	144	143	rx_medium18
rx_full11_hsmc	146	145	rx_medium19
VCC12	148	147	VCC3P3
rx_full12_hsmc	150	149	rx_medium21
rx_full13_hsmc	152	151	rx_medium20
VCC12	154	153	VCC3P3
rxclk_medium	156	155	rx_medium22
rx_full27_hsmc	158	157	rx_medium24
	160	159	VCC3P3

QTH-090-ALTERA

Figure 3-3 Pin-outs of Bank 3 on the HSMC Connector

Table 3-1 shows the pin description of the HSMC connector.

Table 3-1 The pin mappings of the HSMC connector (J3)

HSMC Expansion Connector – J3			
Pin Number	Signal Name	Direction	Function
37	HSMC_TDI	Input	JTAG Test loopback
38	HSMC_TDI	Output	JTAG Test loopback
39	rx_base0	Output	Base output data 0
40	rx_base1	Output	Base output data 1
41	rx_base2	Output	Base output data 2
42	rx_base7	Output	Base output data 7
43	rx_base3	Output	Base output data 3
44	rx_base8	Output	Base output data 8
45	VCC3P3	Power	Power 3.3V
46	VCC12	Power	Power 12V
47	rx_base4	Output	Base output data 4
48	rx_base9	Output	Base output data 9
49	rx_base5	Output	Base output data 5
50	rx_base10	Output	Base output data 10
51	VCC3P3	Power	Power 3.3V
52	VCC12	Power	Power 12V
53	rx_base6	Output	Base output data 6
54	rx_base12	Output	Base output data 12
55	rx_base11	Output	Base output data 11
56	rx_base13	Output	Base output data 13
57	VCC3P3	Power	Power 3.3V
58	VCC12	Power	Power 12V
59	rx_base16	output	Base output data 12
60	rx_base14	output	Base output data 14
61	rx_base18	Output	Base output data 18
62	rx_base15	Output	Base output data 15
63	VCC3P3	Power	Power 3.3V
64	VCC12	Power	Power 12V
65	rx_base19	Output	Base output data 19
66	rx_base17	Output	Base output data 17
67	rx_base20	Output	Base output data 20
68	rxcc4	Input	Camera Control 4
69	VCC3P3	Power	Power 3.3V
70	VCC12	Power	Power 12V
71	rx_base21	Output	Base output data 21
72	rxcc3	Input	Camera Control 3
73	rx_base27	Output	Base output data 27

74	rxcc2	Input	Camera Control 2
75	VCC3P3	Power	Power 3.3V
76	VCC12	Power	Power 12V
77	rx_base26	Output	Base output data 26
78	rxcc1	Input	Camera Control 1
79	rx_base25	Output	Base output data 25
80	rxcc_en	Input	Camera Control enable 1: Enable. 0: Disable
81	VCC3P3	Power	Power 3.3V
82	VCC12	Power	Power 12V
83	rx_base24	Output	Base output data 24
84	rxSerTFG_en	Input	SERTFG Receiver Enable (active low): 0: Enable. 1: Disable
85	rx_base22	Output	Base output data 22
86	rxSerTFG	Output	SERTFG serial data from Camera
87	VCC3P3	Power	Power 3.3V
88	VCC12	Power	Power 12V
89	rx_full14_hsmc	Output	Full output data 14
90	rxSerTC	Input	SERTC serial data from HSTC to Camera
91	rx_medium1	Output	Medium output data 1
92	rxSerTC_en	Input	SERTC Driver Enable. 1: Enable. 0: Disable
93	VCC3P3	Power	Power 3.3V
94	VCC12	Power	Power 12V
95	rx_medium2	Output	Medium output data 2
96	rxclk_base	Output	Receiver base clock
97	rx_medium3	Output	Medium output data 3
98	rxclk_full	Output	Receiver full clock
99	VCC3P3	Power	Power 3.3V
100	VCC12	Power	Power 12V
101	rx_medium4	Output	Medium output data 4
102	rx2SerTC_en	Input	SERTC Driver Enable. 1: Enable. 0: Disable
103	rx_medium5	Output	Medium output data 5
104	rxSerTFG	Output	SERTFG serial data from Camera
105	VCC3P3	Power	Power 3.3V
106	VCC12	Power	Power 12V
107	rx_medium6	Output	Medium output data 6
108	rx2SerTFG_en	Input	SERTFG Receiver Enable (active low):

			0: Enable. 1: Disable
109	rx_medium7	Output	Medium output data 7
110	rx2cc1	Input	Second camera Control 1 (for Dual Base Mode only)
111	VCC3P3	Power	Power 3.3V
112	VCC12	Power	Power 12V
113	rx_medium8	Output	Medium output data 8
114	rx2cc2	Input	Second camera Control 2 (for Dual Base Mode only)
115	rx_medium9	Output	Medium output data 9
116	rx2cc3	Input	Second camera Control 3 (for Dual Base Mode only)
117	VCC3P3	Power	Power 3.3V
118	VCC12	Power	Power 12V
119	rx_medium10	Output	Medium output data 10
120	rx2cc4	Input	Second camera Control 4 (for Dual Base Mode only)
121	rx_medium11	Output	Medium output data 11
122	rx2cc_en	Input	Second camera CC Driver enable pin (for Dual Base Mode only)
123	VCC3P3	Power	Power 3.3V
124	VCC12	Power	Power 12V
125	rx_medium12	Output	Medium output data 12
126	rx_medium0	Output	Medium output data 0
127	rx_medium13	Output	Medium output data 13
128	rx_medium27	Output	Medium output data 27
129	VCC3P3	Power	Power 3.3V
130	VCC12	Power	Power 12V
131	rx_medium14	Output	Medium output data 14
132	rx_medium26	Output	Medium output data 26
133	rx_medium15	Output	Medium output data 15
134	rx_medium25	Output	Medium output data 25
135	VCC3P3	Power	Power 3.3V
136	VCC12	Power	Power 12V
137	rx_medium16	Output	Medium output data 16
138	rx2SerTC	Input	Second camera SERTC (for Dual Base Mode only)
139	rx_medium17	Output	Medium output data 17
140	rx_full9_hsmc	Output	Full output data 9
141	VCC3P3	Power	Power 3.3V
142	VCC12	Power	Power 12V
143	rx_medium18	Output	Medium output data 18

144	rx_full10_hsmc	Output	Full output data 10
145	rx_medium19	Output	Medium output data 19
146	rx_full11_hsmc	Output	Full output data 11
147	VCC3P3	Power	Power 3.3V
148	VCC12	Power	Power 12V
149	rx_medium21	Output	Medium output data 21
150	rx_full12_hsmc	Output	Full output data 12
151	rx_medium20	Output	Medium output data 20
152	rx_full13_hsmc	Output	Full output data 13
153	VCC3P3	Power	Power 3.3V
154	VCC12	Power	Power 12V
155	rx_medium22	Output	Medium output data 22
156	rxclk_medium	Output	Receiver medium clock
157	rx_medium24	Output	Medium output data 24
158	rx_full27_hsmc	Output	Full output data 27
159	VCC3P3	Power	Power 3.3V
160	GND	Power	Power ground
165~172	GND	Power	Power ground

Components

This chapter gives a simple description of the on board components, such as operational mode, signaling standard. For more detailed information you could refer to its datasheet which is available on manufacturer's website or from our provided system CD.

4.1 LVDS 28-Bit Channel Link

Two National Semiconductor LVDS 28-bit channel link chip (DS90CR288A) is installed on the CLR board for receiving LVDS signals from two Camera Link Receiver ports. It converts the LVDS signaling standard into parallel LVCMOS signals, which then connect to the HSMC connector. It can support a shift clock frequency from 20 to 85MHz. Some of the key features are listed below:

- 20 to 85 MHz shift clock support

- Up to 2.38 Gbps throughput

- Four LVDS channels

4.2 3V LVDS Quad CMOS Differential Line Driver

The CLR board features two National Semiconductor DS90LV047A 3V LVDS quad CMOS differential line driver chip for LVCMOS signals to LVDS signals adapting. It is used to transport the control signals to the CameraLink ports. Some of the key features are listed below:

- Four LVDS channels with enable control

- Above 400MHz switch rates

- 3.3V LVCMOS single-ended signaling and +/- 350mV differential signaling

4.3 Operation Mode

With two receiver ports, the CLR supports Base, Dual Base and Medium CameraLink modes. Which mode is in use depends on the connected digital camera. Port J2 is designed to host the base mode CameraLink signals as well as the camera control and serial communication signals. That's, five twisted pairs of LVDS wires carries the Base mode CameraLink signals. Two twisted pairs of LVDS are used for serial communication with the camera and four additional twisted pairs are used

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for camera control. Port J1 is used for Medium mode and Dual Base mode control signals. Five twisted pairs of LVDS wires transport the Medium mode signals. Four twisted pairs of LVDS wires carry the control signals.

Table 4-1 CameraLink Base configuration (J2)

Pin	Signal	Pin	Signal	Remarks
1	Inner shield	14	Inner Shield	
2	CC4-(out)	15	CC4+(out)	Camera Control 4
3	CC3+(out)	16	CC3-(out)	Camera Control 3
4	CC2-(out)	17	CC2+(out)	Camera Control 2
5	CC1+(out)	18	CC1-(out)	Camera Control 1
6	SERTFG+(in)	19	SERTFG-(out)	Serial to Frame Grabber
7	SERTC-(out)	20	SERTC+(out)	Serial to Camera
8	X3+(in)	21	X3-(in)	CameraLink data 3 (base)
9	CLKX+(in)	22	CLKX-(in)	Camera Link clock (base)
10	X2+(in)	23	X2-(in)	CameraLink data 2 (base)
11	X1+(in)	24	X1-(in)	CameraLink data 1 (base)
12	X0+(in)	25	X0-(in)	CameraLink data 0 (base)
13	Inner Shield	26	Inner Shield	

Table 4.2 CameraLink Medium configuration (J1)

Pin	Signal	Pin	Signal	Remarks
1	Inner Shield	14	Inner Shield	
2		15		
3		16		
4		17		
5		18		
6		19		
7		20		
8	Y3+(in)	21	Y3-(in)	CameraLink data 3 (medium)
9	CLKY+(in)	22	CLKY-(in)	Camera Link clock (medium)
10	Y2+(in)	23	Y2-(in)	CameraLink data 2 (medium)
11	Y1+(in)	24	Y1-(in)	CameraLink data 1 (medium)
12	Y0+(in)	25	Y0-(in)	CameraLink data 0 (medium)
13	Inner Shield	26	Inner Shield	

Table 4.3 CameraLink second Base configuration (J1)

Pin	Signal	Pin	Signal	Remarks
1	Inner shield	14	Inner Shield	
2	CC4-(out)	15	CC4+(out)	Camera Control 4
3	CC3+(out)	16	CC3-(out)	Camera Control 3
4	CC2-(out)	17	CC2+(out)	Camera Control 2
5	CC1+(out)	18	CC1-(out)	Camera Control 1
6	SERTFG+(in)	19	SERTFG-(out)	Serial to Frame Grabber
7	SERTC-(out)	20	SERTC+(out)	Serial to Camera
8	X3+(in)	21	X3-(in)	CameraLink data 3 (base)
9	CLKX+(in)	22	CLKX-(in)	CameraLink clock (base)
10	X2+(in)	23	X2-(in)	CameraLink data 2 (base)
11	X1+(in)	24	X1-(in)	CameraLink data 1 (base)
12	X0+(in)	25	X0-(in)	CameraLink data 0 (base)
13	Inner Shield	26	Inner Shield	

Demonstrations

This chapter describes the provided reference designs implemented on CLR in combination with other mother board. These may be the starter point for users to implement application specific codes and give users a comprehensive understanding of how to control CameraLink Standardized peripherals.

We choose the STC-CLC1500 as an example and used in the following demonstrations. User can find its manual in the Datasheet folder on CLR-HSMC system CD. The important specifications are listed below.

- Industry standard camera link interface
- 10-bit digital camera link base configuration
- Resolution of 1360*1024 pixels
- Double speed: 28.636 MHz & Normal speed: 14.318 MHz
- Progressive Scan

5.1 Digital Camera Demonstration for DE4

The example demonstrates a combinational application of digital Camera Link camera and Camera Link Interface Card on DE4 board.

In this demo, we set the camera to work under Double Speed Operation Mode (DIP Switch setting) with internal sync and the others at factory default settings. And the CLR is configured to base mode.

The camera outputs Camera Link Interface specification data to DE4 via the CLR Card. According to Figure 5-1, the CCD_Capture module captures one frame video streams with sync signals, then the RAW2RGB module converts them to RGB format. After that, the frame buffer caches the frame data and sends them to be displayed on a monitor through DVI interface. The output resolution is 1024*768 with a 65MHz pixel clock.

The complete reference design is also located in the CD-ROM attached. Please refer to the following diagram to help you read the code provided.
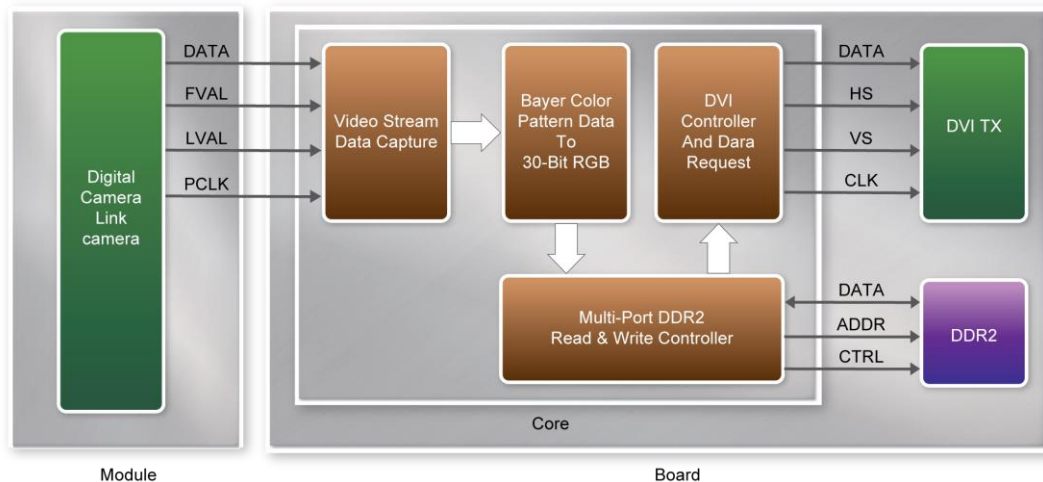
Figure 5-1 Block Diagram of Digital Camera Demonstration for DE4

Locate the project directory from the CD-ROM included and follow the steps below:

Directory: Demonstration / DE4_230/530_CLR

FPGA Bitstream Used: DE4_CLR.sof

1. Ensure the connection is made correctly as shown in **Figure 5-2**. Make sure the CLR Card is connected to **J21 (HSMC PORT B)** and DVI daughter card is connected to **J20 (HSMC PORT A)** of the DE4 board with two **THCB-HMF2** interface cards separately which are bundled in the DE4 kit.

2. Insert the DDR2 memory card into J9 (DDR2 SO-DIMM-1).

3. Connect the DVI TX output of the DVI daughter card to a DVI monitor with a DVI cable, and the camera to **BASE1 (J2)** the CLR card with a Camera Link cable.

4. Copy the directory DE4_230/530_CLR from CLR-HSMC System CD-ROM to the host computer.

5. Download the bitstream (DE4_230/530_CLR.sof) to the DE4 board.

6. Press **BUTTON [0]** on the DE4 board to reset the circuit.

7. User can use the **SW[0]** to set the DVI display mode. When **SW[0]** is set to Off, the DVI will display whatever the camera captures. When set to On, the DVI will display color pattern.
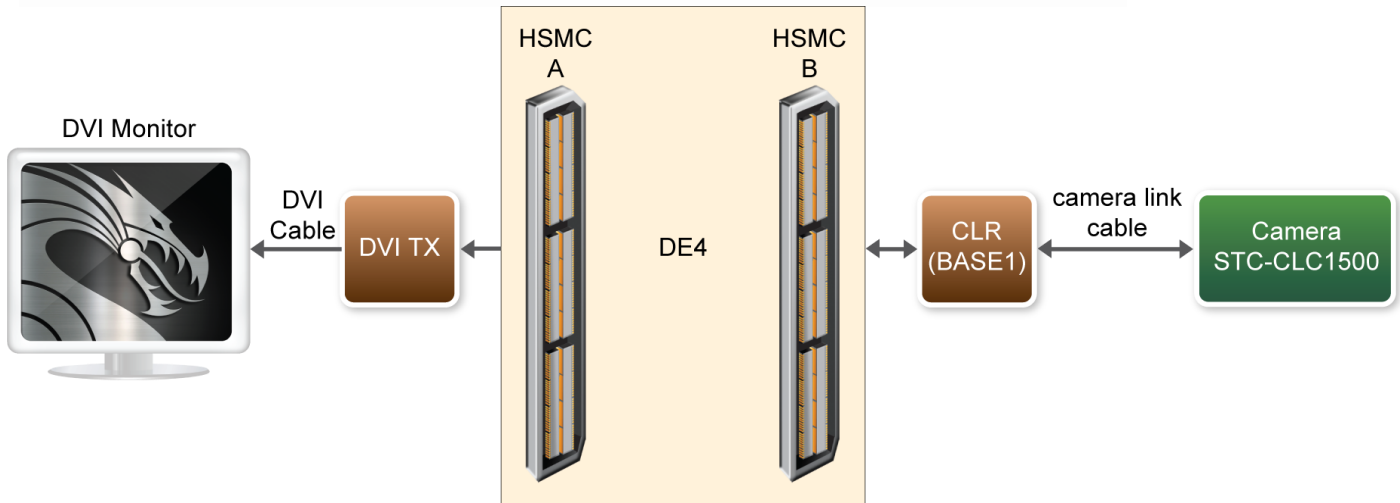
Figure 5-2 The Connection Setup for DE4 Users

5.2 Digital Camera Demonstration for DE3

The example demonstrates a combinational application of digital Camera Link camera and Camera Link Interface Card on DE3 board.

In this demo, we set the camera to work under Double Speed Operation Mode (DIP Switch setting) with internal sync and the others at factory default settings. And the CLR is configured to base mode.

The camera outputs Camera Link Interface specification data to DE3 via the CLR Card. According to Figure 5-3, the CCD_Capture module captures one frame video streams with sync signals, then the RAW2RGB module converts them to RGB format. After that, the frame buffer caches the frame data and sends them to be displayed on a DVI interface monitor. The output resolution is 1024*768 with a 65MHz pixel clock.

The complete reference design is also located in the CD-ROM attached. Please refer to the following diagram to help you read the code provided.
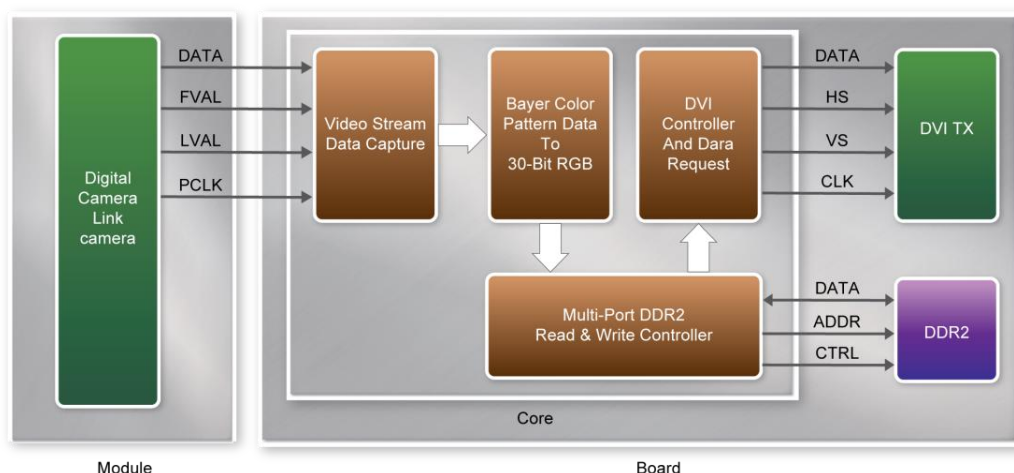
Figure 5-3 Block Diagram of Digital Camera Demonstration for DE3

Locate the project directory from the CD-ROM included and follow the steps below:

Directory: Demonstration / DE3_150/260/340_CLR

FPGA Bitstream Used: DE3_CLR.sof

1. Ensure the connection is made correctly as shown in **Figure 5-4**. Make sure the CLR Card is connected to **J5 (HSTC C)** and DVI daughter card is connected to **J7 (HSTC D)** of the DE3 board both with one **THCB-HFF** interface card which are bundled in the DE3 kit.

2. Insert the DDR2 memory card into **J9 (DDR2 SO-DIMM)**.

3. Connect the DVI TX output of the DVI daughter card to a DVI monitor with a DVI cable, and the camera to **BASE1 (J2)** of the CLR card with a Camera Link cable.

4. Copy the directory DE3_150/260/340_CLR from CLR-HSMC System CD-ROM to the host computer.

5. Download the bitstream (DE3_150/260/340_CLR.sof) to the DE3 board.

6. Press **Button [0]** on the DE3 board to reset the circuit.

7. Users can use the **SW[0]** to set the DVI display mode. When **SW [0]** is set to Off, the DVI will display whatever the camera captures. When set to On, the DVI will display color pattern.
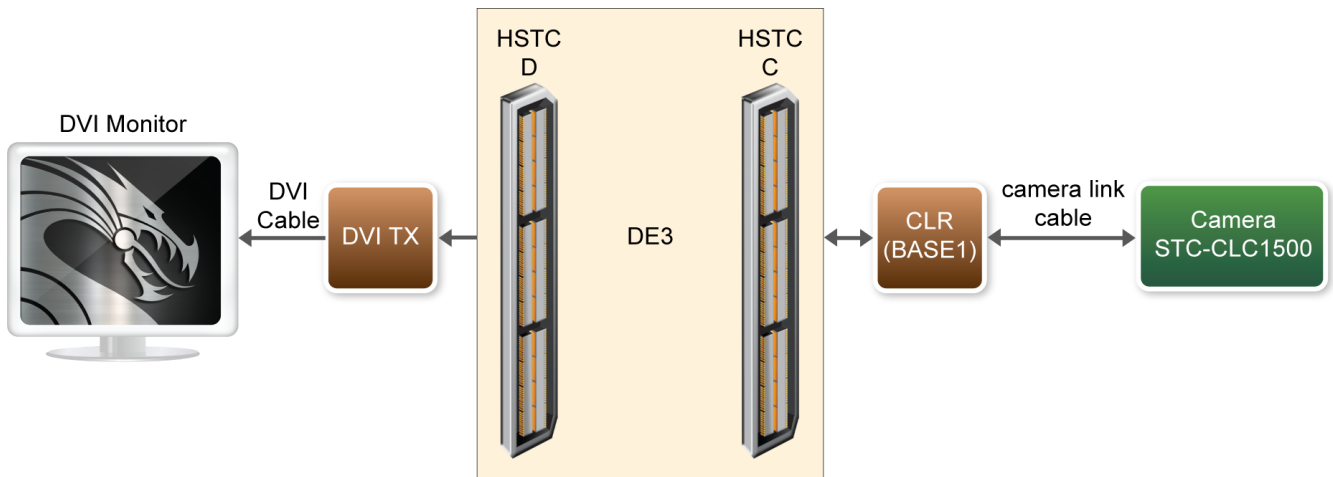
Figure 5-4 The Connection Setup for DE3 Users

5.3 Digital Camera Demonstration for DE2-115

The example demonstrates a combinational application of digital Camera Link camera and Camera Link Interface Card on DE2-115 board.

In this demo, we set the camera to work under Double Speed Operation Mode (DIP Switch setting) with internal sync and the others at factory default settings. And the CLR is configured to dual-base mode.

The camera outputs Camera Link Interface specification data to DE2-115 via the CLR Card. According to **Figure 5-5**, the CCD_Capture module captures one frame video streams with sync signals, then the RAW2RGB module converts them to RGB format. After that, the frame buffer caches the frame data and sends them to be displayed on a DVI interface monitor. The output resolution is 640*480 with a 25MHz pixel clock.

The complete reference design is also located in the CD-ROM attached. Please refer to the following diagram to help you read the code provided.
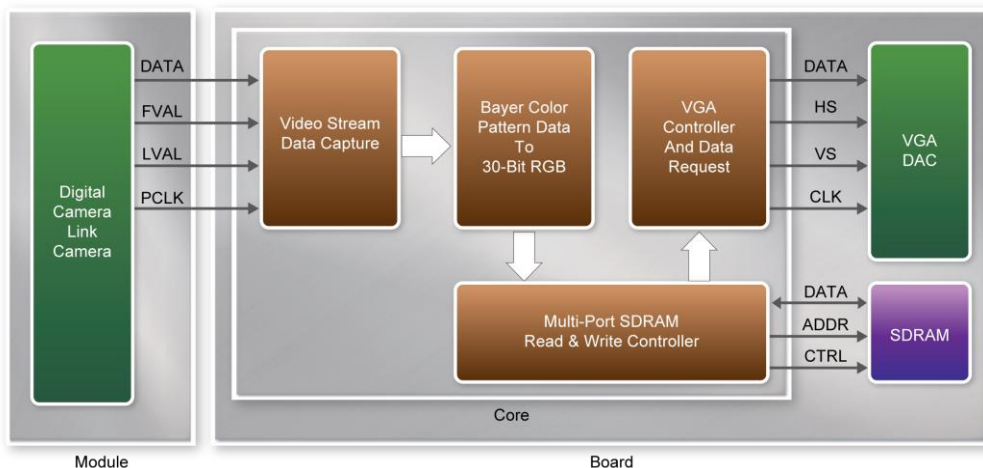
Figure 5-5 Block Diagram of Digital Camera Demonstration for DE2-115

Locate the project directory from the CD-ROM included and follow the steps below:

Directory: Demonstration / DE2_115_CLR

FPGA Bitstream Used: DE2_115_CLR.sof

1. Ensure the connection is made correctly as shown in **Figure 5-6**. Make sure the CLR Card is connected to **JP8 (HSMC)** of the DE2-115 board.

2. Connect the VGA output of DE2-115 board to a VGA monitor, and the camera to **BASE1 (J2)** of the CLR card with a Camera Link cable.

3. Copy the directory DE2_115_CLR from CLR-HSMC System CD-ROM to the host computer.

4. Download the bitstream (DE2_115_CLR.sof) to the DE2-115 board.

5. Set the **SW[0]** to On (upper position) to show the BASE1 camera image (note*).

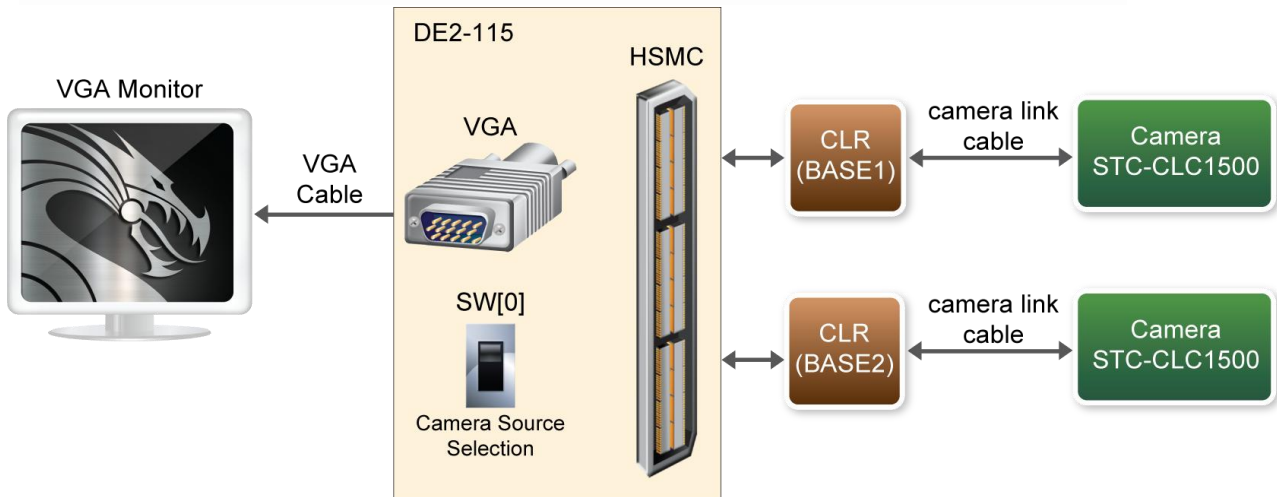6. Press **KEY [0]** on the DE2-115 board to reset the circuit.

Figure 5-6 The Connection Setup for DE2-115 Users

Note: the demo supports dual-base mode, and users can set SW[0] off to show BASE2 camera image.

5.4 Digital Camera with PCI Express Interface for DE4

This example is an extension of the above demo on DE4, we replace the DVI interface monitor with a PC terminal application which communicate with DE4 board via PCIe interface and can perform better real-time display of the video frames. The system block diagram is shown in **Figure 5-7**.

In this demo, we set the camera to work under Double Speed Operation Mode (DIP Switch setting) with internal sync and the others at factory default settings. And the CLR is configured to base mode. The image resolution is 640x480, and the data transfer rate is up to 2.6Gbps.

The complete reference design is also located on the CD-ROM attached. Please refer to the following diagram to help you read the code provided.
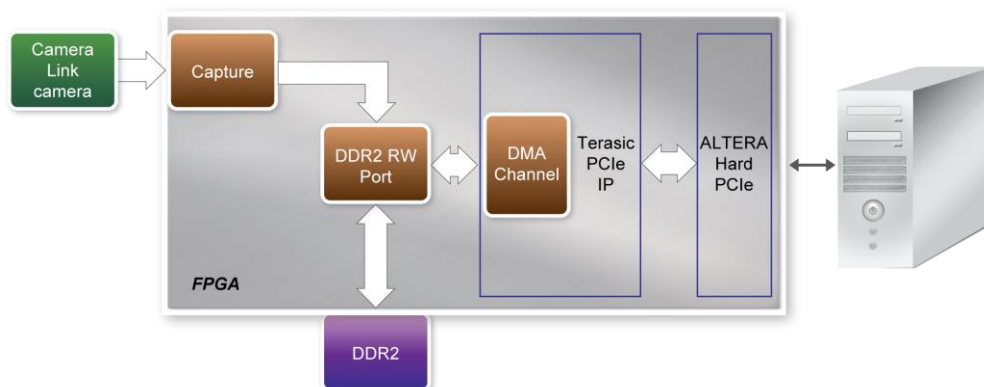

Figure 5-7 The Block Diagram of PCIe Express Application for Camera Link

The Camera Link camera captures and caches the video frames in DDR2 memory via DDR2 Write port. Using ALTERA Hard PCIe and DMA Channel of Terasic PCIe IP, the user application on the PC terminal can access the DDR2 frame buffer via DDR2 Read port.

The user application on PC terminal is developed based on the PCIe Software Stack, which is described in detail in the chapter 6 (PCI Express Reference Design) in DE4 manual. The PCIe vender ID and device ID is 0x1172 and 0xE001, respectively.

Locate the project directory from the CD-ROM included and follow the steps below:

Directory: Demonstration / DE4_230/530_PCIe_CLR

FPGA Bitstream Used: top.sof

PC Application Software: PC/PCIe Monitor.exe

1. Ensure the connection is made correctly as shown in **Figure 5-8**. Make sure the CLR Card is connected to **J21 (HSMC PORT B)** and with two **THCB-HMF2** interface cards which are bundled in the DE4 kit.

2. Insert the DDR2 memory card into J9 (DDR2 SO-DIMM), and turn on the **PCIe X8 detection (SW9)**.

3. Connect a camera to **BASE1 (J2)** of the CLR card with a Camera Link cable.

4. Install the DE4 board on the PC.

5. Copy the directory DE4_230/530_PCIe_CLR from HSMC-CLR System CD-ROM to the host computer.

6. Download the bitstream (top.sof) to the DE4 board.

7. Restart windows.

8. Installed PCIe driver if necessary. The driver is located in the folder PCIe_SDK\Driver

9. Launch PC program Terasic PCIe Monitor.exe, Click **Play** button on the control panel.

10. Press **Button [0]** on the DE4 board to reset the circuit.

Note: the PC Application software development tool is Borland C++ Builder, and the PCI EXPRESS SDKs are provided in PCIe_SDK directory on System CD.
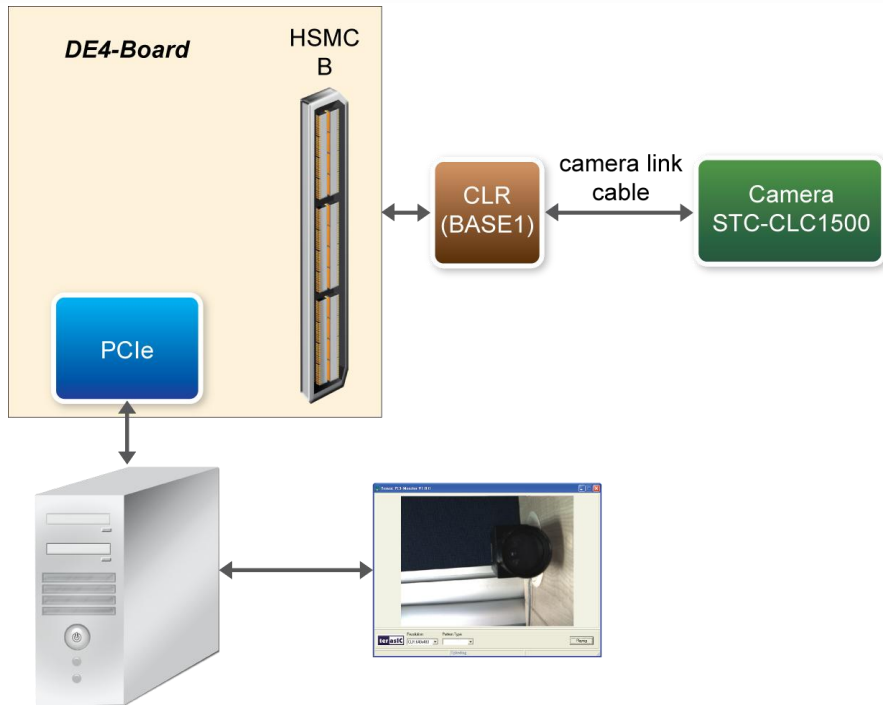
Figure 5-8 Setup for PCI Express Application for Digital Camera Link on DE4

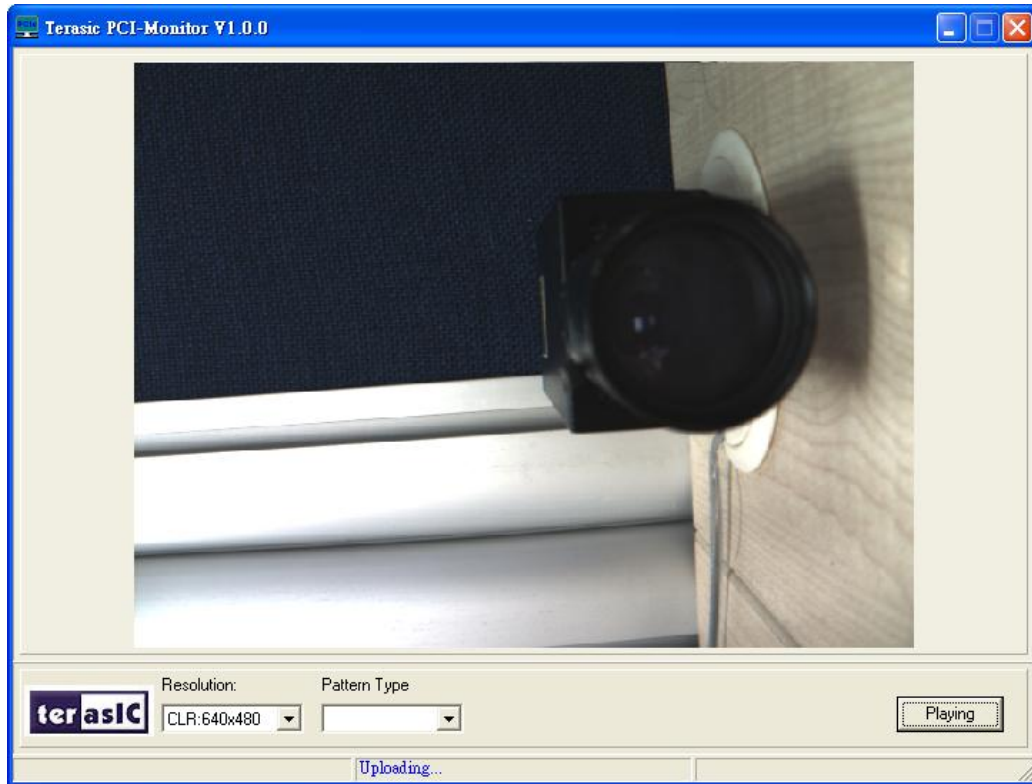Figure 5-9 shows the Terasic PCIe monitor PC program.

Figure 5-9 Terasic PCI-Monitor

Appendix

6.1 Revision History

Version	Change Log
V1.0	Initial Version (Preliminary)
V1.1	Figure 5.6 add BASE2 camera description
V1.2	Add support 2.5 V and 3.3V IO standard description

6.2 Copyright Statement

Always visit CLR_HSMC webpage for new applications.

We will be continuing providing interesting examples and labs on our CLR_HSMC webpage. Please visit www.altera.com or clr.terasic.com for more information.